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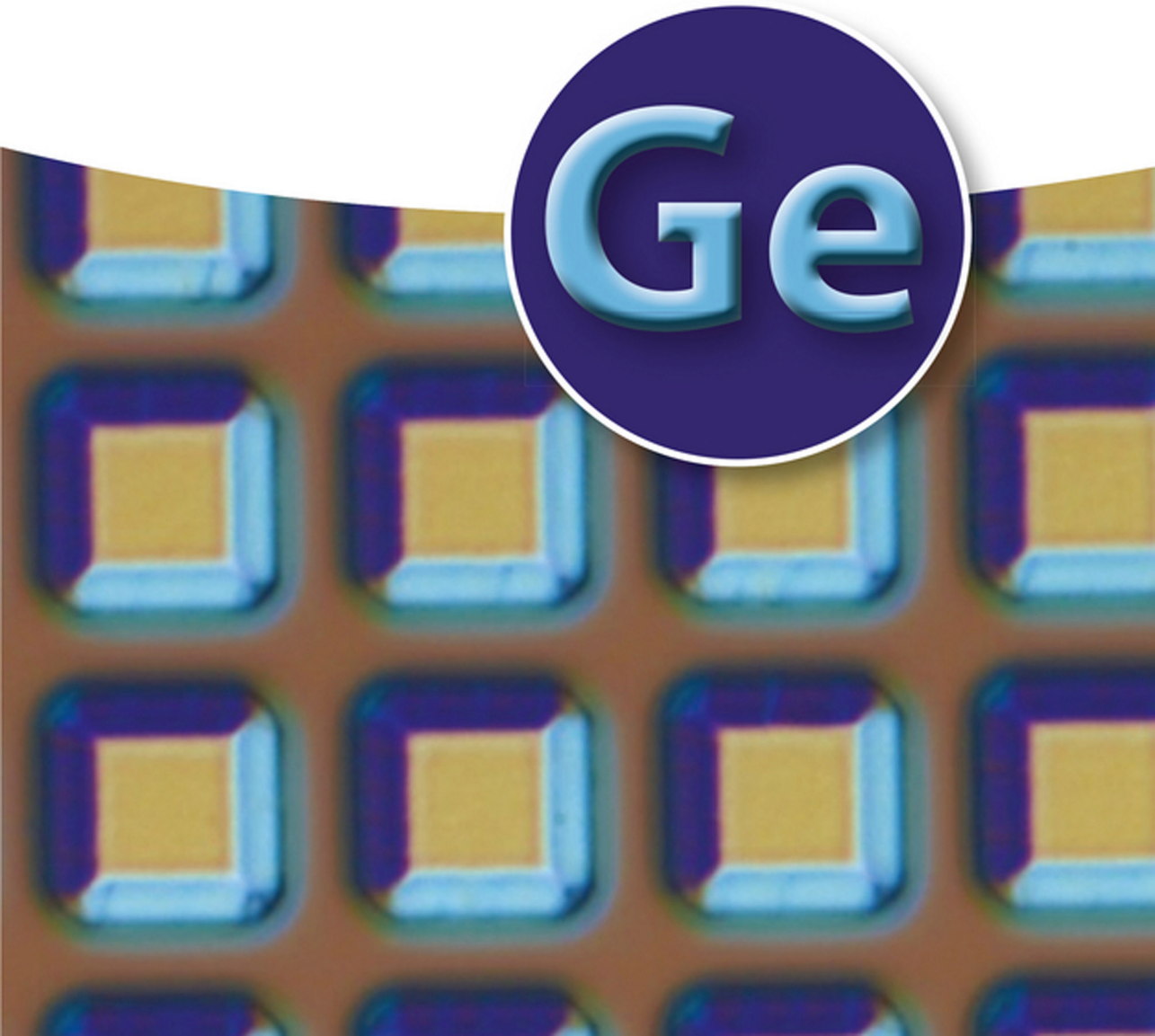

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Preface

The first transistor was made of Ge, and Ge-induced strain provides a scaling path for modern Si-integrated circuits. Ge today has ignited major technology transition from discrete components to integrated photonic circuits. Ge is the material responsible for waveguide-integrated active devices such as photodetectors, modulators, and recently lasers. Monolithic electronic and photonic integration on Si is the key enabler for the next two decades of scaling performance in communication, computing, sensing, and imaging. The emerging interest in the science and engineering of Ge places a very practical, strong demand for solutions that Ge will answer. This book *Photonics and Electronics with Ge* summarizes the current status of understanding of Ge materials science and device physics, and we hope that it will be beneficial to graduate students and researchers working in the field.

Chapters 1 and 2 are intrinsic and extrinsic point defects in Ge. Chapter 1 is on defects in Ge and summarizes the atomic and electronic structures of dopant impurities, point defects, dangling bonds, and hydrogen in comparison with silicon (Si). It focuses especially on the origin of defect levels of vacancies and state-of-the-art self-interstials. Dangling bonds and hydrogen behave differently from these in Si. Chapter 2 is on hydrogen especially on its kinetics such as complex formation and shallow-level passivation in growth cooling. This highlights hydrogen interstitials, dymers, and complexes with intrinsic and extrinsic defects. Chapters 3 and 4 are on epitaxy of Ge. Chapter 3 summarizes Ge-on-Insulator (GeOI) substrate for high-speed nanoelectronics. It describes the comparison of the fabrication technology with hydrogen implantation-induced delamination technique such as SmartCut in terms of defect density. Chapter 4 describes heavy doping of B, P, and C in SiGe by chemical vapor deposition (CVD). The atomic layer doping is well explained based on Langmuir adsorption and reaction scheme. It further marks Si, and/or C atomic layer introduction suppresses impurity diffusion. Chapter 6 is on Ge condensation for GeOI structures. It describes the method and application to the Ge-channel MOSFETs from the aspect of defect reduction in the Ge layer. Chapters 7 – 12 summarize the current status of Ge photonic devices. Chapter 7 is on monolithic integration of Ge photodetectors on Si-on-Insulator (SOI) platform and views the next generation of electronics and photonics integration. Chapter 8 is on Ge photodetectors and high-volume deployment for

optical links among computers. Foundry-based production proves Ge photodetectors to be one of the primary enablers and building block for the high-speed computing and communication. Chapter 9 is on Ge-based electroabsorption (EA) modulators. It describes Franz–Keldysh modulator based on Ge, which is one of the promising modulators for Si photonics in terms of high bandwidth, high energy efficiency, and relatively wide operation wavelength window. Chapter 10 is on strain engineering of Ge, Si, and GaAs on SOI structures. It describes dynamic control of bandgap of these materials in terms of strain and potential application to wavelength tuning for dense wavelength division multiplexing (DWDM). Chapter 11 is on light emission from Ge quantum dots in photonic crystal structures. Strong enhancement of light emission is demonstrated depending on the quality (Q) factor and volume. Chapter 12 is on Ge lasers. It reviews historical aspect, theoretical modeling, band engineering approach of Ge lasing in terms of optical pumping and electrical injection. The group IV laser will enhance monolithic integration of photonics and electronics on Si CMOS platform.

Two decades ago, as the Internet ushered in the Information Age with optical fiber networks, it would have been hard to imagine the connected world of today. Today, it is equally hard to imagine the changes that Ge and photonic integration will bring to the Information Age during the next two decades.

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20 March 2015 at MIT

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1
Defects in Germanium

Justin R. Weber, Anderson Janotti, and Chris G. Van de Walle

1.1
Introduction

Many properties of solids are strongly affected by the presence of defects or impurities. In semiconductors, impurities are routinely incorporated in small quantities as a means of controlling the electrical conductivity. This practice, referred to as doping, is at the heart of modern solid-state device design, where *p*-*n* junctions are used in a myriad of different applications such as diodes, transistors, light emitters, and solar cells. A *p*-*n* junction is an interface between two semiconductor regions of different conductivity type: *p*-type and *n*-type. *n*-type semiconductors contain impurities referred to as donors, which contribute electrons to the empty conduction-band states of the semiconductor that lead to *n*-type conductivity. In a *p*-type semiconductor, the presence of impurities called acceptors causes electrons to be removed from the filled valence-band states. These removed electrons leave behind mobile charged electronic vacancies in the valence band (referred to as holes), which induce *p*-type conductivity.

In addition to intentionally incorporated impurities, native point defects are also present. These are defects that are intrinsic to a given material, such as vacancies (missing atoms), self-interstitials (additional atoms), or antisites (a cation sitting on an anion site or vice versa in a compound semiconductor). Such native point defects are typically electrically active, and can lead to compensation, that is, a reduction in the conductivity that one aims to achieve by incorporating dopant impurities. Native point defects are involved in self-diffusion [1], but also play a critical role in dopant diffusion, because the motion of impurities is typically assisted by vacancies or self-interstitials [2–5]. Point defects may also act as carrier traps or be involved in degradation.

It is therefore crucial to understand the nature and origin of point defects in order to control their formation and concentration. This is particularly important because germanium has emerged as a promising material for use in the channel of novel complementary metal-oxide Semiconductor (CMOS) devices. Compared to silicon CMOS, germanium offers higher channel mobilities and lower voltage operation due to its significantly smaller band gap. However, problems exist,

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Table 1.1 Bulk properties of silicon and germanium.

Property	Silicon	Germanium
Band gap (eV)[a)]	1.15	0.75
Electron mobility ($cm^2\ (V \cdot s)^{-1}$)[b)]	1500	3900
Hole mobility ($cm^2\ (V \cdot s)^{-1}$)[b)]	470	1900
Electron effective mass (m_e)[c)]	1.08	0.55
Hole effective mass (m_e)[c)]	0.56	0.37
Static dielectric constant[b)]	11.7	16
Lattice constant (Å)[a)]	5.43	5.66
Bulk modulus (GPa)[a)]	98	75
Cohesive energy (eV/atom)[a)]	4.63	3.85

a) $T = 0\,K$ data from Ref. [6].
b) $T = 300\,K$ data from Ref. [7].
c) Density-of-states effective mass ($T = 300\,K$) from Ref. [8].

particularly in *n*-channel MOS field-effect transistors (FETs), which are likely caused by the presence of defects near the semiconductor/dielectric interface, such as germanium dangling bonds (DBs).

Throughout this chapter, we will occasionally compare results for germanium with those for silicon. Such comparisons are meaningful not only because germanium is frequently integrated with silicon in devices, but also because of the similarities between the two semiconductors. Germanium, like silicon, is a semiconductor with the diamond crystal structure. Both are indirect semiconductors with similar properties, as shown in Table 1.1. However, the conduction-band minimum (CBM) in germanium occurs at the *L*-point in the Brillouin zone, while the CBM occurs near the *X*-point in silicon. In addition, germanium has a significantly higher hole mobility compared to silicon, making it a desirable choice for a number of applications.

1.2 Methods for Studying Defects and Impurities

1.2.1 Experimental Techniques

A number of experimental techniques exist for studying point defects and impurities.

Electron spin resonance (*ESR*) is one of the most powerful techniques for the study and identification of defects in semiconductors [9]. It provides information about the chemical identity of the atoms in the vicinity of the defect, as well as about the symmetry of the defect. ESR relies on the presence of unpaired electrons. In cases where the stable ground-state configuration of the defect is not

paramagnetic, optical excitation can often be used to generate a metastable charge state with a net spin density. Optically detected magnetic resonance (ODMR) is a variant of the technique that can offer additional information about defect-induced levels in the band gap [10]. The ability to directly compare measured hyperfine parameters with calculated values for specific defect configurations allows for an explicit identification of the microscopic structure [11, 12].

Vibrational spectroscopy can be applied to defects or impurities that give rise to local vibrational modes (LVMs), whose frequencies and polarization contain information about the chemical nature of the atoms involved in the bond as well as the bonding environment [13]. Comparisons with calculations [14] can again facilitate the identification of the observed defect and its structure.

Positron annihilation spectroscopy (*PAS*) [15] can be used to identify point defects and measure their concentration, but it is mostly sensitive to negatively charged defects and typically limited to detection of vacancies.

The electronic structure of defects can be studied with electrical techniques such as *temperature-dependent Hall measurements* [16] or *deep-level transient spectroscopy* (*DLTS*) [17]. Optical levels can be observed in *photoluminescence, absorption, or cathodoluminescence experiments*[18].

Finally, we mention *perturbed angular correlation spectroscopy* (*PACS*), which is a type of γ-ray spectroscopy that is used to study hyperfine interactions on probe nuclei introduced into a crystal. Point defects near the probe nuclei modify internal fields, allowing the determination of defect association energies, migration barriers and formation energy differences between defects within a crystal [19, 20]

1.2.2
First-Principles Calculations

Modern first-principles calculations can provide deep insight into the nature of defects and impurities in semiconductors. Owing to a substantial increase in available computational power as well as in the development of novel algorithms, first-principles techniques have achieved an unprecedented level of predictive power, accuracy, and the ability to treat systems with an increasingly large number of atoms. Such methods allow calculating the energetic properties of solids at the microscopic level and the investigation of both the atomic and electronic structure of defects and impurities. As mentioned in Section 1.2.1, first-principles methods allow calculating observables that can be directly compared with experiments, and also quantities that are difficult to extract directly from experiments such as electronic wavefunctions, microscopic charge densities, defect formation energies, and local atomic relaxations.

Most state-of-the-art first-principles (or *ab initio*) calculations for defects and impurities in solids are based on density functional theory (DFT) [21]. DFT seeks to determine the ground-state properties of the many-body electronic system present in solids. DFT in the Kohn–Sham (KS) scheme [22] provides an approximate solution to this problem by formulating it as a single-particle problem in which the electrons move in an effective potential that is composed of the

Coulomb potential due to the atomic nuclei; the classical Hartree potential due to all of the other electrons in the system; and a so-called exchange-correlation potential (V_{XC}), which captures the quantum-mechanical many-body interactions. An exact expression for V_{XC} is not known, but approximations such as the local density approximation (LDA) or generalized gradient approximation (GGA) have been shown to provide very good descriptions of structural properties [23, 24]. Within the LDA, V_{XC} is assumed to depend only on the *local* charge density [22]; the GGA additionally takes local variations of the charge density into account [25, 26]. Within the LDA, V_{XC} is assumed to have the value corresponding to a homogeneous electron gas with a density equal to the local charge density; values for the homogeneous electron gas are obtained with high accuracy from quantum Monte Carlo simulations [27, 28].

DFT with traditional functionals such as the LDA and GGA has been very successful in describing the many properties of molecules and solids, but it has significant shortcomings in its description of electronic band structures, an issue commonly referred to as the band-gap problem, because the band gap of semiconductors and insulators is significantly underestimated. Sometimes this underestimation is so severe that an LDA or GGA calculation actually produces a zero band gap, that is, a metal, which is the case with germanium [29].

A variety of approaches have been proposed to overcome this problem. The most rigorous are based on many-body perturbation theory, the lowest order approximation being the GW approximation [30]. The GW approach is generally regarded as the method of choice for computing excitation spectra of weakly correlated systems, but it still has limitations: it is computationally expensive for calculating the large supercells needed to study defects and impurities, and no practical scheme is currently available for self-consistently calculating energetics and forces (and thus atomic relaxations), rendering it difficult to study cases where large structural relaxations occur [31, 32]. In addition, The GW calculations typically use wave functions calculated with LDA or GGA as input, and problems may arise when defect states do not lie within the DFT-calculated band gap.

A number of approximate correction schemes also exist, the simplest being a "scissors operator," that is, a rigid shift of conduction bands and possibly conduction-band-derived states to bring the fundamental gap in line with the experimental value. More sophisticated approaches based on the extrapolations of certain parameters have been proposed but these introduce additional uncertainties [33]. Pseudopotentials are typically used in conjunction with DFT calculations in order to avoid solving an all-electron problem. The construction of pseudopotentials allows some flexibility in the choice of parameters, and modified pseudopotentials have been successfully implemented for corrections of the DFT band structure [34].

Aside from the band gap, some other features of DFT band structures calculated with LDA or GGA may be inaccurate: semicore states (such as the Ge 3*d* states) are underbound and hence too close to the valence-band states. This error contributing to the band-gap underestimation as *p*-*d* repulsion pushes the valence-band

maximum (VBM) upward and closer to the CBM. In the DFT+U scheme, an orbital-dependent potential is applied to the semicore d states. This potential adds an extra Coulomb interaction (U) to such states, and lowers their energetic position on an absolute energy scale. The lowering of the d states shifts the VBM downward (due to p-d coupling) and opens up the band gap. This leads to a partial opening of the band gap, but the band gap is not *fully* corrected as it still suffers from underestimation due to other DFT-inherent causes such as self-interaction errors. Still some improvement in the band structure occurs, and such DFT+U calculations have been applied to defects in germanium [35, 36].

It would be desirable to have a methodology that stays within DFT and retains its capability to efficiently calculate energetics and forces, while improving the band structure. Novel functionals have been developed that have proven successful in achieving these goals. Hybrid functionals essentially mix the standard GGA functional with a certain amount of exact exchange, as would be obtained from the Hartree–Fock method. The two most common implementations of this approach were developed by Perdew, Ernzerhof, and Burke (PBE0) [37–40] and by Heyd, Scuseria, and Ernzerhof (HSE) [41, 42]. Both include 25% Hartree–Fock exact exchange, but the HSE formalism truncates the contributions from exact exchange at a certain length, which allows for more accurate descriptions of metallic systems and also results in a reduction of computational demands.

1.3 Impurities

1.3.1 Shallow Dopants

The most common dopant impurities for silicon and germanium are group-III elements as p-type dopants and group-V elements as n-type dopants. A shallow dopant is characterized by a small ionization energy. For example, arsenic in germanium introduces an extra electron resulting from arsenic having five valence electrons (as opposed to four for germanium). The atomic electronic level corresponding to this arsenic state lies well above the CBM of germanium, and, therefore, the extra electron drops to the bulk CBM of germanium, that is, an extended electronic state. Within that state, the electron is Coulombically attracted to the positive As center, a situation described by hydrogenic effective mass theory. The energy difference between the ground state of this hydrogen-like system (modified by the dielectric constant and the effective mass of the host material) determines the ionization energy. Table 1.2 lists the ionization energies for a number of common dopants in silicon and germanium. Table 1.2 shows that ionization energies are significantly smaller in germanium as compared with silicon, which can be attributed to its larger dielectric constant and smaller effective masses.

Another important characteristic of dopant impurities is their solubility, which determines how easily dopants can be incorporated. Table 1.3 lists the solid solubility limits for some common dopants in silicon and germanium.

Table 1.2 Dopant ionization energies in silicon and germanium.

Dopant impurity	Type	Silicon (meV)	Germanium (meV)
B	*p*-type	45	10
Al	*p*-type	67	10
Ga	*p*-type	72	11
In	*p*-type	160	11
P	*n*-type	45	12
As	*n*-type	54	13
Sb	*n*-type	39	9.6

Source: Data from Ref. [8].

Table 1.3 Dopant solid solubility limits in silicon and germanium.

Dopant impurity	Type	Silicon (10^{20}cm^{-3})	Germanium (10^{20}cm^{-3})
B	*p*-type	6.0	–
Al	*p*-type	0.2	4.0
Ga	*p*-type	0.4	5.0
P	*n*-type	15.0	–
As	*n*-type	19.0	1.9
Sb	*n*-type	0.7	0.1

Source: Data from Ref. [43].

Dopants can be incorporated in a variety of ways. Sometimes this is accomplished during the growth of the material itself; in other cases, in separate treatments. The two most common methods include diffusion and ion implantation. In diffusion techniques, a high concentration of dopant atoms is first introduced onto the surface of the semiconductor by coating the semiconductor surface with a dopant-containing layer, and using elevated temperatures to cause the dopant atoms to diffuse into the semiconductor. In ion implantation, an ion beam bombards the semiconductor substrate, implanting dopants into the material as well as simultaneously damaging the substrate, thus requiring a post-implantation anneal.

In all cases, controlling the spatial distribution of dopants is a challenge. Some applications require an even distribution of dopants throughout the semiconducting material, but state-of-the-art devices typically require precise positioning of dopant atoms over small length scales (on the order of nanometers). This is typically accomplished using ion implantation, followed by a rapid thermal anneal. The diffusivity of many dopants is mediated by native defects in the semiconductor [2, 4]. In the case of germanium, many impurities (such as arsenic) diffuse faster than germanium itself, which may be attributed to both the electrostatic attraction between the impurities and native defects [2, 4]. Figure 1.1 illustrates the higher diffusivity of arsenic compared with self-diffusion in germanium. Other impurities such as boron and silicon diffuse slower than

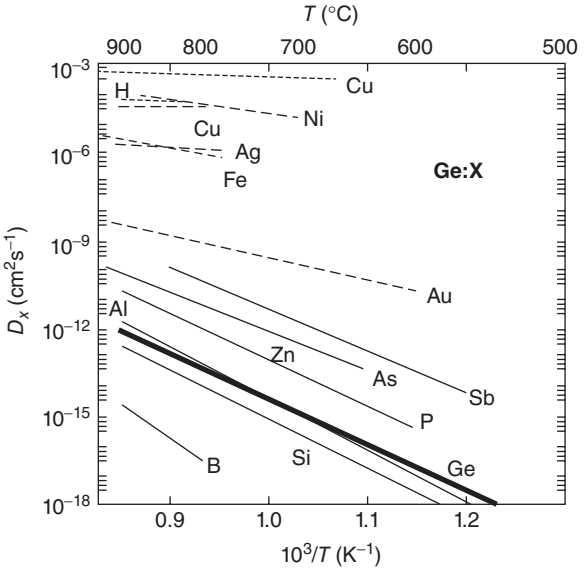

Figure 1.1 Temperature dependence of the diffusion constant of foreign atoms in Ge (thin lines) compared with self-diffusion (thick line). Solid lines represent diffusion data of elements that are mainly dissolved on substitutional lattice sites. Long-dashed lines (– –) indicate hybrid elements, which are mainly dissolved on substitutional sites, but diffuse in an interstitial configuration via the dissociative mechanism. The short-dashed lines (- - - -) indicate elements that are mainly interstitially dissolved. The upper short-dashed line shows the diffusivity deduced for interstitial copper. Figure courtesy of Ref. [2]

the self-diffusion in germanium, which can happen if the impurity atoms are electrostatically repelled from native defects [2].

Impurities can diffuse via substitutional or interstitial sites. Native defects can assist this diffusion through a variety of mechanisms. For example, if a vacancy and substitutional impurity atom are attracted to one another (to minimize local strain, or by electrostatic interaction), they can diffuse to form a complex. This pair can then dissociate and subsequently reform along a different direction, leading to long-range migration [4, 44]. Self-interstitial defects can also assist impurity diffusion. This requires the self-interstitial atom and impurity atom to stay spatially localized and not dissociate. When the self-interstitial (paired with the impurity) diffuses one atomic site, it can create a local lattice distortion that causes the impurity to follow [44]. There are also dissociative mechanisms by which substitutional impurity atoms can diffuse through interstitial sites [44]. Such diffusion involves the creation and destruction of vacancies as the impurity moves from substitutional to interstitial sites. Finally, we mention the *kick-out* mechanism, which is assisted by self-interstitials: the impurity is kicked out of a substitutional site, migrates interstitially, and then rejoins a substitutional site by kicking a bulk lattice atom into an interstitial position. Therefore, in order to fully understand dopant or

impurity incorporation (and diffusion), it is clearly essential to study the behavior of native defects.

1.3.2 Hydrogen

Hydrogen is a ubiquitous impurity that is present in most growth and processing environments, and is easily incorporated in materials. In semiconductors, interstitial hydrogen usually acts as an amphoteric impurity, that is, it behaves as a donor in *p*-type material and as an acceptor in *n*-type material [45, 46]. This implies that hydrogen counteracts the prevailing conductivity, and will have a tendency to form complexes with dopant impurities [47]. In germanium, however, hydrogen exhibits a less usual behavior where it is always negatively charged [48, 49]. The reason for this behavior is linked to the fairly high position of the germanium VBM on an absolute energy scale [50]. Combined with the fact that the electronic defect level associated with interstitial hydrogen is approximately constant on an absolute energy scale, this explains why hydrogen in silicon is amphoteric while in germanium hydrogen is exclusively an acceptor. This behavior has important consequences for hydrogen's ability to passivate defects in germanium, as will be discussed in Section 1.4.4.

1.4 Intrinsic Defects

We have already mentioned that native defects can interact with impurity atoms and determine their diffusivity. In addition, native point defects can be electrically active and introduce defect levels within the band gap. Such energy levels can degrade device performance, as will be discussed in Section 1.4.4. In bulk germanium, native defects can take the form of vacancies (missing atoms) or interstitials (extra atoms). At interfaces, native defects can be characterized by a lack of consistent bonding across the interface; such defects are referred to as DBs.

1.4.1 Vacancies

1.4.1.1 Electronic Structure

When a vacancy is created in germanium, an atom is removed and four bonds are broken. The remaining DBs can be represented as sp^3 orbitals (Figure 1.2). The interaction of these orbitals produces a symmetric state (commonly referred to as a_1) and three degenerate states (commonly referred to as t_2). Depending on the occupancy of these states (as determined by the charge state of the vacancy), the degeneracy of the t_2 states can be split by Jahn–Teller distortions. These t_2 states can also be split by strain or the presence of another defect or impurity atom nearby. An assessment of the stability of different charge states requires a discussion of the formation energy of the vacancy.

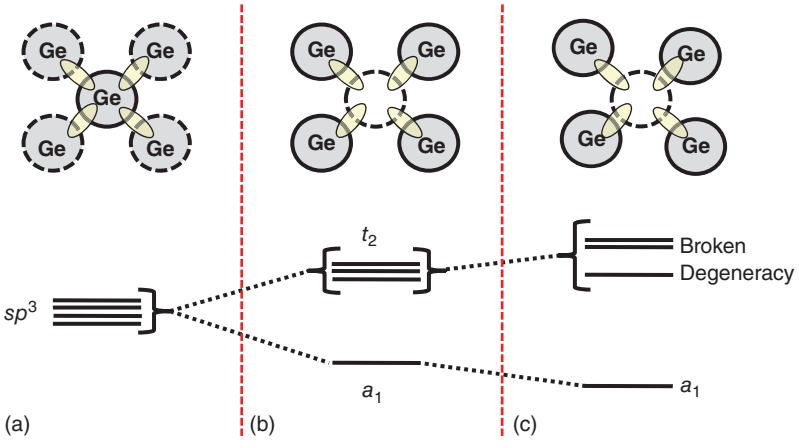

Figure 1.2 Electronic structure of the vacancy in germanium. (a) sp^3 bonding orbitals in germanium. (b) Symmetric a_1 and degenerate t_2 defect states for the vacancy in germanium. (c) Symmetry breaking can split the t_2 states due to strain, Jahn–Teller distortion, or nearby defects.

1.4.1.2 Formation Energy

The formation energy is a key quantity for characterizing defects in solids. In the dilute regime and assuming thermal equilibrium, the formation energy (E^f) of a defect is related to its concentration through a Boltzmann relation [24]:

$$C = N_0 \; e^{-E^f/k_B T}, \tag{1.1}$$

where N_0 is the number of sites the defect can incorporate on, including the number of possible configurations per site, k_B is the Boltzmann constant, and T is the temperature. For a vacancy in charge state $q(V^q_{Ge})$, the formation energy is defined as follows [24]:

$$E^f[V^q_{Ge}] = E_{tot}[\text{Ge} : V^q_{Ge}] - E_{tot}[\text{Ge} : \text{bulk}] + \mu_{Ge} + q\varepsilon_F. \tag{1.2}$$

The E_{tot} terms are the total energies of the germanium crystal with and without the defect. For the defect, a supercell geometry is used. Note that inclusion of spin polarization is essential to ensure correct occupation of the defect states. μ_{Ge} is the chemical potential, representing the energy of the reservoir in which the germanium atom that was removed from the solid was placed. In the case of an elemental solid such as germanium, this is simply the energy per atom of a bulk germanium crystal. Sometimes this is presented as placing the germanium atom that was removed on the surface of the material; this increases the number of bulk atoms by one, leading to the same conclusion that the reference energy is equivalent to that of a bulk germanium atom.

When the vacancy is in charge state q, q electrons have been removed from the defect, and these electrons have been placed in a reservoir with energy ε_F, that is, the electron chemical potential or (in semiconductor language) the Fermi level. Typically, ε_F is referenced to the bulk VBM. The Fermi level in Eq. (1.2) is a

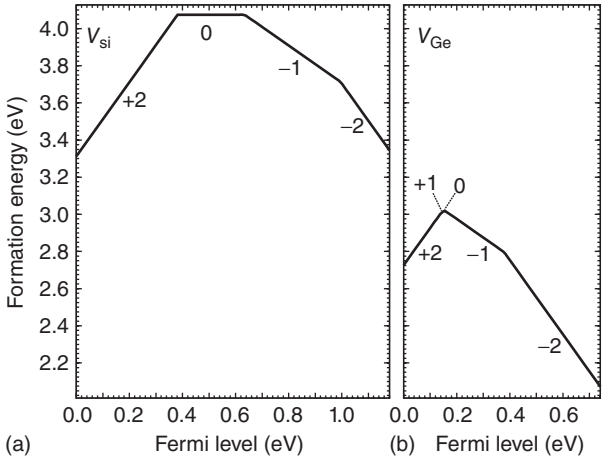

Figure 1.3 Formation energy of vacancies in silicon (a) and in germanium (b) as calculated with hybrid density functional theory [51]. Only the lowest energy charge state is shown for each value of the Fermi level.

variable. In practice, the Fermi level is of course fixed to a value that is determined by local charge neutrality, taking into account all point defects and all impurities (in all possible charge states) that are present in the material. However, we will see that it is instructive to examine the formation energy of the defect as a function of ε_F, allowing us, for instance, to examine what would happen in *p*-type (ε_F close to the VBM) versus *n*-type material (ε_F close to the CBM).

We, therefore, plot the formation energy as a function of ε_F, as illustrated in Figure 1.3 for both Si and Ge. The values shown here were obtained with the hybrid density functional technique described in Section 1.2.2, using the HSE functional. For calculational details we refer to Ref. [51]. For a given value of the Fermi level, only the lowest energy charge state is shown, and the slope of the line segment corresponds to the charge of the defect. We note that the concentration of higher energy charge states is exponentially attenuated (Eq. (1.1)).

Figure 1.3 shows that germanium vacancies have a significantly smaller formation energy than silicon vacancies. Consequences, particularly for diffusion, will be discussed in Section 1.4.1.5.

1.4.1.3 Defect Levels

The kinks in the curve indicate transitions between different charge states of the defect. The Fermi-level positions at which these occur determine the so-called charge-state transition levels (q/q'), which can be derived from the calculated formation energies:

$$(q/q') = -\frac{E^f(\mathrm{D}^q;\varepsilon_F = 0) - E^f(\mathrm{D}^{q'};\varepsilon_F = 0)}{q - q'} \ , \tag{1.3}$$

Table 1.4 Charge-state transition levels associated with the vacancies in silicon and germanium as calculated with hybrid density functional theory [51].

Transition Level	Silicon (eV)	Germanium (eV)
(+2/+1)	–	0.14
(+1/0)	–	0.15
(+2/0)	0.38	–
(0/ − 1)	0.63	0.16
(−1/ − 2)	1.00	0.38

where $E^f(\mathrm{D}^q; \varepsilon_F = 0)$ is the formation energy of the defect D in charge state q when the Fermi level is at the VBM. For $\varepsilon_F < (q/q')$, the defect is stable in charge state q, while for $\varepsilon_F > (q/q')$, the defect is stable in charge q'. These transition levels are also sometimes referred to as thermodynamic transition levels, and can be probed using experimental techniques such as DLTS, in which the final charge state is able to fully relax to its corresponding equilibrium atomic configuration after the charge-state transition.

Table 1.4 lists the charge-state transition levels for the vacancies in germanium and silicon. Table 1.4 and Figure 1.3 show that the (+2/+1), (+1/0), and (0/ − 1) charge-state transition levels in germanium are very close in energy. PACS measurements have found the (0/ − 1) transition level to be located at 0.2 ± 0.04 eV above the germanium VBM [52, 53], in good agreement with the result in Table 1.4. The (−1/ − 2) level is calculated to be 0.38 eV above the VBM in germanium. A vacancy-related charge-state transition level at 0.33 eV has been detected with DLTS [54].

Physical insight into the formation of the +2, +1, 0, and −1 charge states and the corresponding transition levels can be obtained by considering the single-particle states introduced in Section 1.4.1.1. We illustrate these single-particle states in Figure 1.4. In the neutral charge state of the vacancy, four electrons (one from each germanium sp^3 orbital) are available to fill the vacancy-induced single-particle KS states. Two electrons go into the a_1 state (below the VBM) and two are left to occupy the spin-up channel of the t_2 states, leading to a spin-1 configuration. The +1 charge state of the vacancy is obtained by removing one electron from the t_2 states, leading to a configuration with spin 1/2. Removing a second electron leads to the +2 charge state and a spin-0 configuration. The a_1 states, which are well below the VBM, always remain occupied, and hence the +2 charge state is the lowest achievable charge state of the vacancy. Upon adding one additional electron to obtain the −1 charge state, there are 5 electrons: 2 in the a_1 state, and 3 in the spin-up channel of the t_2 states, which are thus occupied with one electron each. This leads to a spin-3/2 configuration. We thus see that starting from +2, the +1, 0, and −1 charge states are obtained by adding one, two, or three electrons to the spin-majority channel of the t_2 states. These electrons go into different orbitals, and apparently inter-orbital repulsion is quite weak, explaining why the (+2/+1),

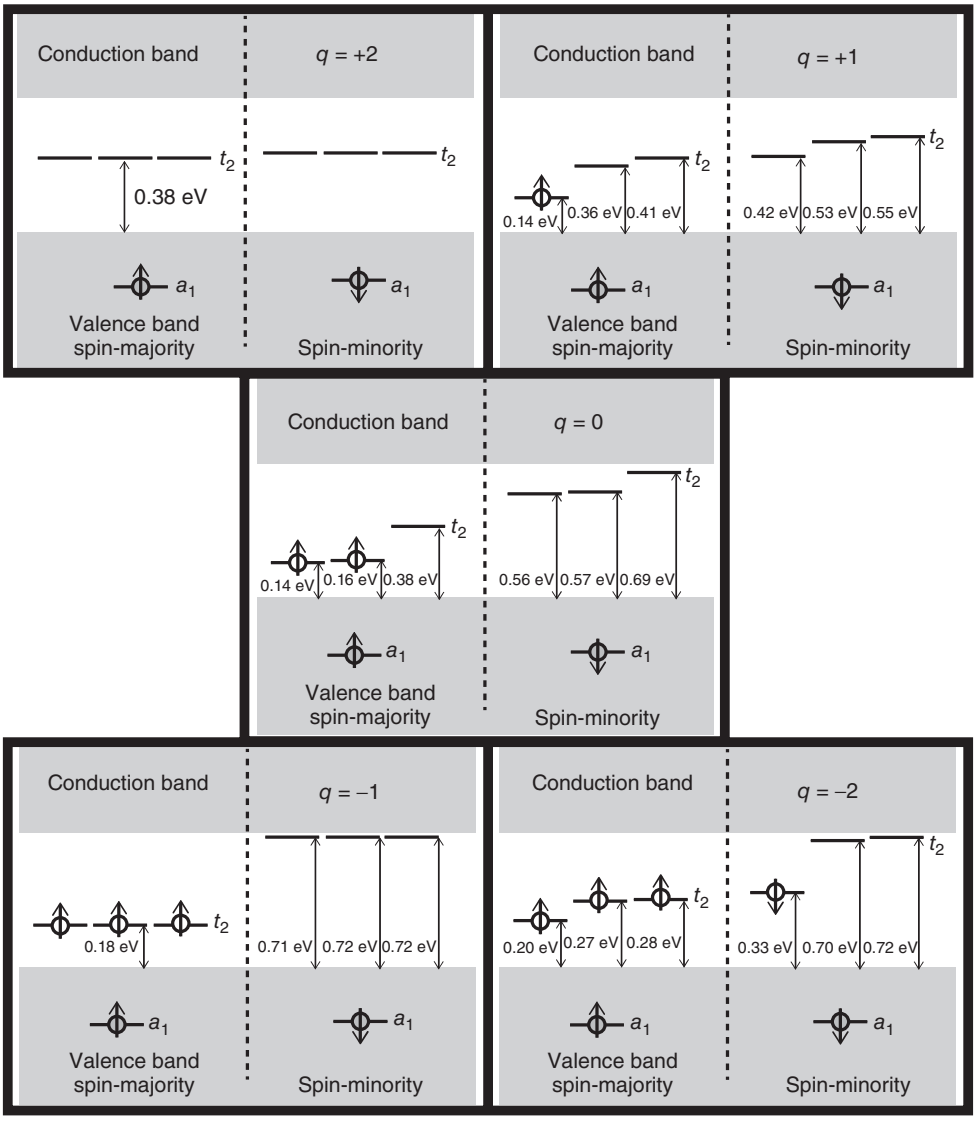

Figure 1.4 Kohn–Sham states for the +2 to −2 charge states of the vacancy in germanium. These results were obtained through spin-polarized hybrid density functional theory calculations [51].

(+1/0), and (0/ − 1) charge-state transition levels are very close together in energy, as seen in Table 1.4.

To obtain the −2 charge state, however, an electron must now be added to the spin-minority channel associated with the t_2 states. This now causes intra-orbital electron–electron repulsion (apparently much stronger than inter-orbital repulsion) between the two electrons in the t_2 state that is doubly occupied; a significant

rearrangement of the single-particle states occurs and explains the large separation between the $(0/-1)$ and $(-1/-2)$ charge-state transition levels, as seen in Table 1.4).

The results shown in Figure 1.3 and Table 1.4 are in broad agreement with other density functional calculations for vacancies in germanium reported in the literature [35, 36, 55]. The discrepancies that do occur can be mainly attributed to the different approximations made within the DFT framework. In the study by Fazzio *et al*. [55] modifications were made to the germanium pseudopotential, while Śpiewak *et al*. [35] employed LDA+U and Tahini *et al*. [36] used GGA+U. In addition, the studies by Fazzio *et al*. [55] and Tahini *et al*.[36] did not consider spin polarization, which is essential to obtain a correct occupation of single-particle states.

1.4.1.4 Comparison with Silicon

Figure 1.3 shows that the +1 charge state is not stable in silicon, while the +1 charge state of the vacancy in germanium is stable over a small but finite range of Fermi levels. The calculations for silicon [51] show that the +1 charge state is never thermodynamically stable. Such a situation, where the stable charge state as a function of Fermi level jumps from +2 to 0, is referred to as a negative−U transition [56]. Experimentally, the fact that the +1 charge state of the silicon vacancy is not stable has indeed been observed using DLTS [57].

The relative spacing of the charge-state transition levels of the vacancy is very different in silicon and germanium (Figure 1.3). The difference can be mainly attributed to the different behavior of the neutral charge state. In germanium, the atomic structures of the +2, +1, 0, and −1 charge states are quite similar, that is, the atomic relaxations do not drastically change as electrons are added to the t_2 spin-up states. But in silicon, the neutral charge state exhibits distinctly larger relaxations, indicative of extensive rebonding (probably induced by silicon's smaller lattice constant) and resulting in a lowering of the energy of this charge state relative to the other charge states. This Jahn – Teller distortion lowers the two occupied t_2 eigenvalues with respect to the unoccupied one and is responsible for the much larger spacing of the $(+1/0)$ and $(0/-1)$ transition levels in silicon compared to germanium.

1.4.1.5 Diffusion

Self-diffusion in germanium is known to be largely governed by vacancies [1, 4, 5]. The diffusion activation energy is the sum of formation energy and migration barrier. A migration barrier of 0.1 eV was calculated for the vacancy in germanium [58]. The formation energy is a function of Fermi level. For modest doping levels (below $\sim 5 \times 10^{18}$ cm^{-3}) the material is close to intrinsic at the temperatures of interest for diffusion, and under those conditions the vacancy will likely be in a −1 charge state, with a formation energy of $\sim$ 2.9 eV (Figure 1.3). Combined with the migration barrier, this leads to an activation energy for self-diffusion of 3.0 eV, in remarkable agreement with the experimental values of 3.1 eV [1].

Assuming that vacancies are also a major contributor to self-diffusion in silicon, the same exercise leads to a migration barrier of 0.5 eV [59] and a formation energy of 4.1 eV for the neutral charge state (Figure 1.3), resulting in an activation energy of 4.6 eV—again in good agreement with the experimental value of 4.8 eV [60].

We note that that the value of the formation energy of the vacancy depends on the Fermi level (Figure 1.3), and therefore doping may impact self-diffusion, particularly at high doping levels. This has indeed been observed experimentally [61].

1.4.2 Self-Interstitials

Self-interstitials are formed when extra atoms are added to the crystal. Self-interstitials can exist in a variety of atomic configurations, illustrated in Figure 1.5.

The split interstitial is formed by placing two atoms on a single lattice site. The orientation of these two atoms defines the type of split interstitial. In both silicon and germanium, the <110> orientation (illustrated in Figure 1.5a) is the lowest in energy for stable charge states of the split-interstitial [62–65]. The hexagonal interstitial is formed by placing a germanium atom on a sixfold coordinated interstitial site, while the tetrahedral interstitial is located on a fourfold-coordinated site. Intermediate structures can be formed by placing an interstitial atom at a

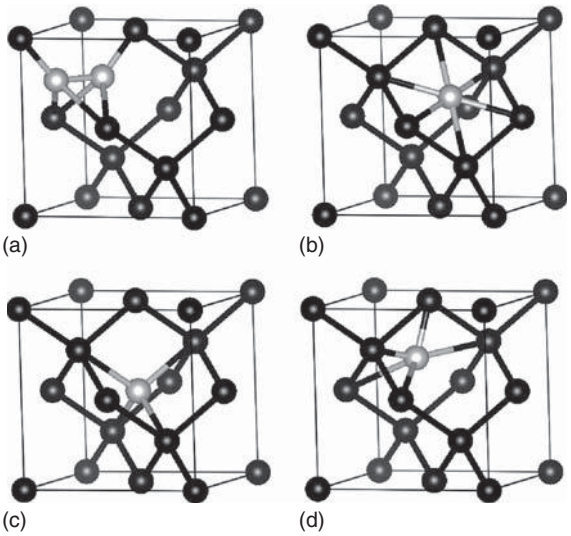

Figure 1.5 Atomic configuration for various types of self-interstitial defects in germanium. The types are defined as: (a) split interstitial, (b) hexagonal interstitial, (c) tetrahedral interstitial, and (d) open cage structure formed by a bond-center interstitial atom relaxing outward toward the hexagonal site (distorted hexagonal structure). Black atoms indicate bulk-like atoms. Gray atoms indicate the interstitial atom(s).

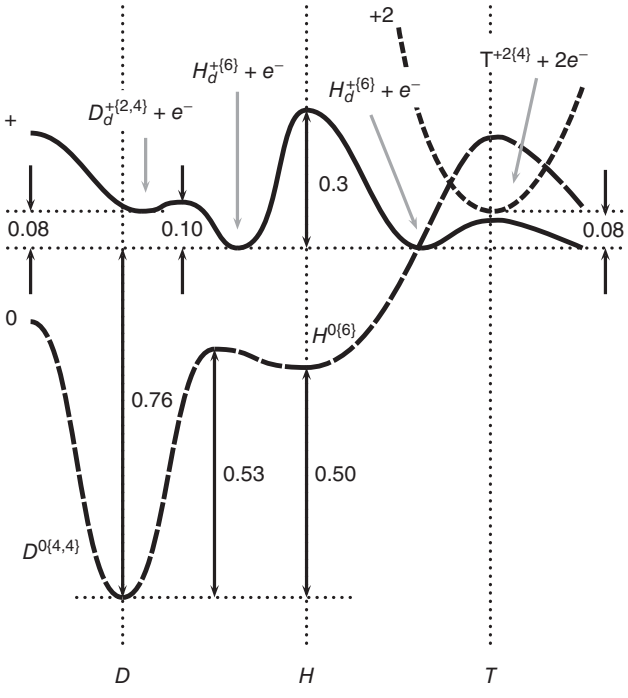

Figure 1.6 Configuration-coordinate diagram for the self-interstitial in germanium. *D* denotes the split-interstitial, *H* the hexagonal interstitial, and *T* the tetrahedral interstitial. Figure courtesy of Ref. [63].

bond-center location and then allowing the structure to relax toward the tetrahedral or hexagonal configuration [66].

Because the interstitial can exist in different atomic configurations, it is possible for the lowest-energy atomic configuration of one charge state to be different from that in a different charge state. First-principles calculations based on DFT-LDA combined with nonlinear core corrections for the germanium *d* states [63] indicated that the neutral charge state is stable in the split-interstitial configuration, while the +2 charge state is stable in the tetrahedral configuration. The +1 charge state is most stable in an open cage structure similarly to Figure 1.5d (distorted hexagonal configuration) [63, 66].

Because of this stability in different atomic configurations, it is important to understand the barriers associated with the various interstitial configurational transformations. Figure 1.6 illustrates these barriers, as well as the lowest energy configurations for the 0, +1, and +2 charge states. We see that the barriers associated with metastable states for the neutral and +1 charge states are very small, indicating that it is unlikely that interstitials will become trapped in metastable states.

First-principles calculations based on DFT-LDA consistently find the (+1/0) charge-state transition level to be very close to the VBM [64, 65]. Experimentally,

PACS data suggests that the self-interstitial produces a transition level in the vicinity of the CBM [52, 53]. The origin of this particular transition has been debated [64, 65], but the most likely assignment is the $(0/-1)$ transition. We note that calculations for self-interstitials to date have been performed only with DFT-LDA [64, 65], making conclusive assignments difficult due to the band-gap problem.

In germanium, the self-interstitial is a less important defect than the vacancy because of its significantly higher formation energy [4, 5]. Dopant diffusion in germanium is predominantly mediated by vacancies [4, 5].

1.4.3 Dangling Bonds

1.4.3.1 Electronic Levels

Vacancies and self-interstitials are point defects that occur within the bulk of a germanium crystal. At an interface with another semiconductor or insulator, deviations from perfect coordination may occur, leading to DBs. Figure 1.7 illustrates a schematic atomic configuration for a DB at a germanium/germanium-oxide interface.

A number of first-principles calculations have been performed for DBs in silicon [68, 69] and germanium [48, 51, 69]. Figure 1.8 displays the results for DB defect levels from Ref. [51], again comparing silicon and germanium.

Calculations for DBs in silicon place the $(+/0)$ level at an energy of about 0.1–0.2 eV above the VBM, and the $(0/-)$ level at about 0.6–0.8 eV, indicating that the neutral DB would be stable over quite a large range of Fermi levels within the band gap [51, 69] (Table 1.5). This agrees with EPR experiments [71–73] that probe the neutral charge state of the DB of an MOS capacitor, finding that the neutral charge state is stable over a 0.5 eV range within the silicon band gap [71].

Calculations for DBs in germanium lead to results for the DB levels that agree to within about 0.2 eV [51, 69], with the defect levels occurring near the germanium

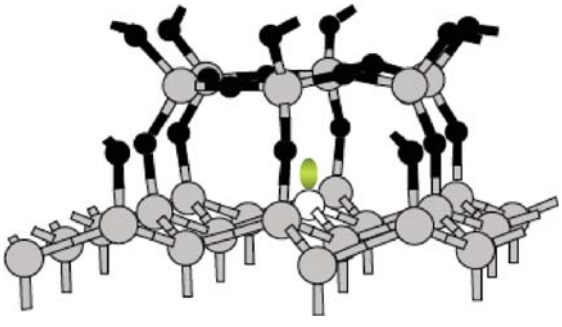

Figure 1.7 Schematic representation of a dangling bond at a germanium/germanium-oxide interface. Gray atoms represent germanium, black atoms oxygen, and the white atom the germanium atom with the DB. Figure courtesy of Ref. [67].

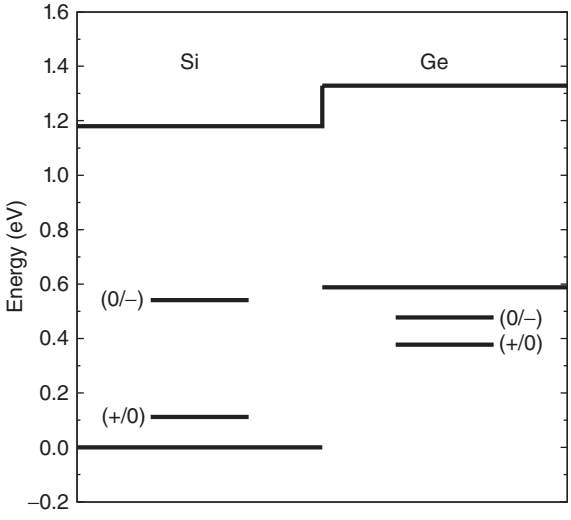

Figure 1.8 Charge-state transition levels for dangling bonds in silicon and germanium as calculated with hybrid density functional theory [51]. The connected bottom lines indicate the VBM for silicon and germanium, while the connected top lines indicate the CBM for these materials. The alignment of the band structures is based on the calculated valence-band offset of 0.6 eV [70]. The short lines indicate the charge-state transition levels associated with the dangling bonds [51].

Table 1.5 Charge-state transition levels associated with the dangling bonds in silicon and germanium as calculated with hybrid density functional theory [51].

Transition Level	Silicon (eV)	Germanium (eV)
$(0/-1)$	0.10	−0.11
(+1/0)	0.55	−0.21

VBM. Some of the calculations place the (0/−) level of the DB below the VBM [48, 51], while others place it just above the VBM [69]. Although the quantitative difference is quite small, this leads to qualitatively different results: in one case, the DB can only be stable in a negative charge state (and thus not be observable by ESR, which requires a neutral charge state), while in the other, different charge states are in principle possible—although the authors of Ref. [69] argued that the concentration of neutral DBs would be small. ESR experiments have been unsuccessful at detecting DBs at germanium/oxide interfaces [74], indicating that the concentration of neutral DBs is undetectably small.

Additional experimental information is provided by ESR studies of Si_{1-x} Ge_x/SiO_2 interfaces [75, 76], by analyzing the interfacial ESR signal as a function of the germanium concentration (x). The results were used to provide an estimate of where the germanium DB defect level would lie if referenced to the silicon band

gap, resulting in a value 0.35 ± 0.10 eV above the silicon VBM [76]. If we use the data in Figure 1.8 and assume that the germanium DB level remains constant on an absolute energy scale as the alloy concentration is changed—a reasonable assumption for a highly localized state such as the DB—we can use the valence-band offset between silicon and germanium (0.6 eV [70]) to estimate the position of the germanium DB level in pure silicon; this estimate leads to a value for the germanium DB $(0/-1)$ level of 0.49 eV above the Si VBM, in reasonable agreement with the experimental determination. If anything, experimental results point to an even lower position of the germanium DB than what is depicted in Figure 1.8.

Therefore, by combining existing experimental data with current state-of-the-art *ab initio* calculations, we obtain a complete and consistent picture of the DB in germanium. Comparing these results with those for the silicon DB (as presented in Figure 1.8), we expect DBs to behave very differently in germanium-based devices than they do in silicon-based devices. In Section 1.4.4 we discuss this in detail.

1.4.4 Impact on Devices

Compared with silicon, germanium CMOS devices still lag in performance. *p*-channel MOSFETs show acceptable performance but exhibit an undesirable positive threshold voltage shift [77]. *n*-channel MOSFETs suffer from low channel mobilities and on-state currents [78–80]. These problems are likely caused by the presence of defects, such as germanium DBs, near the semiconductor/dielectric interface. In Section 1.4.3.1 we discussed that the levels of the DB in germanium are likely to be below the VBM, causing it to always be negatively charged. DB defects near an interface will therefore give rise to negative fixed charge, creating serious problems for devices that rely on the formation of an electron channel (such as *n*-channel MOSFETs) [81]. Even for *p*-channel devices, such fixed charge will induce undesirable carrier scattering, as well as a positive threshold voltage shift, which has also been experimentally observed [77].

DBs are known to also occur at silicon/oxide interfaces. As illustrated in Figure 1.8), silicon DBs induce defect levels within the silicon band gap, which, in principle, also act as carrier traps in MOS devices. In silicon, hydrogen is very effective at passivating interfacial DB defects [82]. Hydrogen can bind to the silicon DB, forming an Si–H bond that has no defect levels in the band gap.

However, as discussed in Section 1.3.2, hydrogen behaves very differently in germanium compared to silicon. In silicon, hydrogen is an amphoteric impurity, but in germanium, hydrogen acts exclusively as an acceptor and is thus always negatively charged [48, 49]. Hydrogen interstitials will thus be electrostatically repelled from DBs in germanium, and will not effectively passivate DB defects. This is consistent with experimental observations showing that hydrogenation is ineffective in reducing interface-state densities at germanium/oxide interfaces [74]. Given the inability of hydrogen to passivate DB defects, alternative passivation strategies will need to be explored for germanium.

1.5 Summary

We have discussed the atomic and electronic structure of dopant impurities, point defects, DBs, and hydrogen in germanium, along the way comparing with silicon. We showed how results from first-principles calculations can help in interpreting experimental results and aid in developing a complete understanding of defects. Specifically, we discussed the origin of defect levels introduced by germanium vacancies, comparing to silicon. For the germanium interstitial, we illustrated the various configurations and charge states for which it can be stable. DBs as well as hydrogen exhibit qualitatively different behavior in silicon versus germanium. This leads to a number of problems for germanium-based devices, and the need for novel passivation schemes.

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2
Hydrogen in Ge[1)]

Jörg Weber

2.1
Introduction

Hydrogen is an omnipresent element, which is easily incorporated into semiconductors during growth or processing. Three charge states H^+, H^0, and H^- make hydrogen a reactive impurity which interacts with many different types of impurities and intrinsic defects. Depending on the host crystal, hydrogen acts as a donor, an acceptor, or as an amphoteric impurity. Formation of H_2 molecules is the simplest form of self-passivation of hydrogen. The existence of the molecules was proposed very early on by theory and experiment. Today, studies on the quantum mechanical properties of ortho- and para-hydrogen have opened the view on fundamental nuclear spin relaxations in the lattice. Passivation of electrical active defects like donors, acceptors, or recombination centers is one of the major applications of intentional hydrogen incorporation in semiconductors and is extensively used today, for example, in the improvement of photovoltaic cells. However, although undesirable, electrically active centers can be created at the same time by hydrogen.

Crystalline Ge has been the preferred host for most of the early studies on defects in semiconductors. The research was driven by the need for an improved Ge quality. In particular, the search for sensitive γ-ray detectors has led to the growth of large Ge crystals in H_2-atmosphere. The early work on hydrogen in Ge stimulated very careful research on defects in very low concentrations. Later, due to the increasing technological relevance of Si in semiconductor technology, most experimental and theoretical studies on hydrogen were performed in Si. Today, the behavior of hydrogen is best understood in Si and generally the understanding was successfully transferred to other semiconductors. However, there are astonishing differences found in some materials, which cast doubt on the general behavior of H in different hosts. Contrary to the amphoteric behavior of H in Si, hydrogen generates only shallow donor states in ZnO and InN; in GaN acceptor interaction with hydrogen leads to the formation of passive and active acceptor–hydrogen

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complexes. In diluted group III-N-V semiconductors hydrogen causes a surprising shift of the semiconductor band gap.

Several excellent reviews on hydrogen in semiconductors are available today [1–7]. However, the reader should be aware that, usually, reviews reflect the personal preference of the author and that till today this field is rapidly developing and assumptions and models can quickly change.

Hydrogen in semiconductors is the ideal candidate for local vibrational mode (LVM) spectroscopy. By replacing hydrogen with its stable isotope deuterium an unsurpassed relative mass ratio of 1 : 2 is achieved, which leads to a relative frequency shift of $\sim \sqrt{2} : 1$. The high spectral resolution of FTIR (Fourier Transform Infra Red) spectroscopy has helped to unravel many of the LVMs of hydrogen complexes. In most cases hydrogen is present only in low concentrations and the detection of electrical activities is only possible with highly sensitive techniques. "Deep Level Transient Spectroscopy" (DLTS) [8] and also "Photothermal Ionization Spectroscopy" (PTIS) [9] have contributed to the study of electrical active defects in detail.

However, without the power of most advanced theory and computational techniques, the field of hydrogen in semiconductors would have never reached the present level of understanding. Indeed, this area can be regarded as a prototype of a stimulating and fruitful interplay between theory and experiment.

This report will be restricted to the discussion on the results of hydrogen in crystalline Ge. First, a short summary on the present understanding of isolated H in Ge will be provided. The second part will address the behavior of H-dimers in Ge, while the third part provides the results on the interaction of H with shallow dopants. This part also includes new evidence for the detrimental influence of hydrogen on the Schottky barrier in p-type Ge.

2.2 Properties of Hydrogen in Ge

2.2.1 Incorporation of Hydrogen

The first detailed studies of H in Ge were performed in the so- called "ultra-pure" Ge. For γ-ray detectors crystalline Ge with highest purity was needed. The ultra-pure Ge was achieved by growing crystals in hydrogen atmosphere [10–12]. Cooling from the melting point to room temperature (RT) resulted in total H-concentrations in the bulk of up to 10^{15} cm^{-3}. Most of the hydrogen is electrically inactive and precipitates in clusters or defect-complexes [13, 14].

The diffusion and solubility of H in crystalline Ge was studied at high temperatures by effusion measurements. The permeation rate through a thin Ge slab was found to vary as the square root of the H_2 gas pressure, which indicated that at these temperatures the hydrogen exists in the germanium lattice as hydrogen atoms or ions. Similar to Si, high diffusivity and low solubility were detected for H

in Ge [15, 16]. Extrapolating the diffusion data to 350 °C provides however values about 200 times larger compared to those which were experimentally observed [17, 18]. This reduced, apparent diffusivity was related to a strong pairing of mobile hydrogen, resulting in hydrogen molecules or other defect-complexes [12].

The introduction of hydrogen from plasma sources is a convenient way to introduce hydrogen at lower temperatures in Si [19]. Special care is needed in selecting the plasma parameters and the position of the samples with respect to the plasma to reduce surface damage. In particular, treatments in a remote hydrogen plasma, which separates the sample from the plasma, showed no plasma surface damage after hydrogenation [20].

A first systematic study of deuterium introduction in ultra-pure Ge from an rf-plasma showed a quite different behavior compared to Si [21]. Only at the surface high concentrations of deuterium could be detected by SIMS. Even long treatments did not increase the hydrogen concentration above the detection limit of $\geq 10^{17}$ cm^{-3} in the bulk. At much lower concentrations of several 10^{14} cm^{-3} the authors were able to detect hydrogen in the bulk, which was bound in Cu–H complexes. Effusion measurements on plasma-treated highly doped p-type Ge samples yield an out-diffusion of hydrogen already at 200 °C, much lower than in Si (350–400 °C) [22]. The hydrogen content in the sample decreases with higher sample temperatures in the plasma. At 250 °C all hydrogen is located on or near the sample surface even for exposure times as long as 20 h. It was suggested that the Ge surface acts as an effective diffusion barrier or binding center for atomic hydrogen, which prevents the incorporation of significant concentrations inside the bulk material [22]. However, under very similar plasma conditions it was possible to form in the bulk of the Ge samples transition metal (TM) complexes with hydrogen in concentrations of ~2 to 5×10^{12} cm^{-3} [23].

Proton implantation at low temperatures was performed to study interstitial hydrogen and several hydrogen complexes with radiation defects [24–27].

Hydrogen could be incorporated electrochemically into Ge from phosphoric acid at RT, but the technique also generated a thin disordered, highly hydrogenated layer at the surface [28]. Treatment at 213 °C resulted in a similar low bulk concentration of Cu–H complexes, as compared with a sample treated at the same temperature in the plasma [21].

Wet chemical etching at RT is the ideal technique in Si to incorporate hydrogen without additional defect or damage formation; in addition changes in the defect structure due to thermal annealing are avoided. No penetration of hydrogen after wet chemical etching of n-type Ge is detected. In p-type Ge an increase of negatively charged hydrogen close to the sample surface after etching in CP4 or KOH at RT is reported [29].

2.2.2 Isolated Hydrogen

For the three electronic levels of isolated hydrogen (H^+, H^0, H^-) in semiconductors, theory predicts a negative-U ordering with the donor level H(+/0)

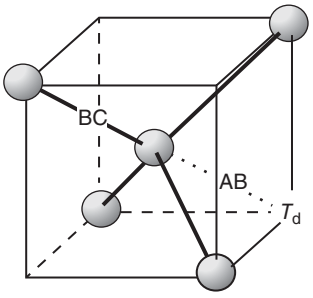

Figure 2.1 The local positions for the hydrogen ground state in the diamond lattice: the bond-center site (BC) for H^+ and the anti-bonding site (AB) for H^-.

energetically above the acceptor level H(0/−). The neutral state H^0 is, in thermal equilibrium, not the lowest energy state in the crystal. As the Fermi-level rises, the charge state of H changes from positive to negative. The change in charge state is connected with a change in the lattice position. The hydrogen donor state is located at the bond-center (BC)-site and the acceptor state at or near the T-site in the anti bonding configuration (AB). Figure 2.1 provides a schematic presentation for the locations of isolated H in the diamond lattice. Therefore, transfer from the positive to the negative charge state involves not only the capture or emission of electrons or holes but also the crossing of potential barriers between the two sites. Depending on the energies of the electronic transitions and the potential barriers, the neutral charge state can form a metastable state with long lifetimes.

The Fermi-level position $\varepsilon(\pm)$ also called the occupancy level at which the concentrations of the positive and negative charge states are equal was calculated for various semiconductors [30, 31]. A general feature evolved from the calculations, $\varepsilon(\pm)$ could serve as a universal alignment in different semiconductor hosts with respect to the vacuum level. From the known band offsets the position of the hydrogen occupancy level can be calculated. There is no report on a direct experimental determination of $\varepsilon(\pm)$.

In agreement with the universal alignment and with more recent calculations the $\varepsilon(\pm)$ level in Ge is situated approximately 50 meV below the valence band edge [32, 33]. According to these calculations, H^- should be the stable equilibrium configuration for all Fermi-level positions. Hydrogen in Ge would exhibit non-amphoteric behavior with a shallow acceptor level, which compensates the n-type conductivity and possibly enhances the p-type conductivity. Only non-equilibrium conditions could lead to the generation of H^+ or H^0 in Ge. Qualitatively, similar results were calculated in Ref. [34]. However, these authors determine the occupancy level well above the valence band edge at E_v +0.29 eV. Under these conditions hydrogen would still be an amphoteric impurity in Ge.

Experiments on isolated hydrogen are difficult to perform, due to the negative-U properties and the high reactivity of hydrogen. The position of the donor- and acceptor-levels can only be studied at low temperatures and under non-equilibrium conditions.

Detailed information about the atomic positions of hydrogen in different semiconductors came from muon spin research (μSR) [35]. This technique involves the

implantation of spin polarized positive muons (μ^+), which interact with defects in the lattice. Muonium (Mu), a positively charged muon with an electron ($\mu^+ - e^-$), is seen as a hydrogen isotope with one-ninth the mass of the proton. One should however be careful in comparing the dynamical properties of Mu and H due to their quite different masses. The decay of muons is detected via the associated positron emission. The low-temperature implantation process leads to a frozen-in non-equilibrium distribution of various metastable sites and charge states.

The μSR measurements in Ge revealed Mu^+ at the BC-site and Mu^- close to the tetrahedral (AB) site. Influence of temperature and light allowed to determine the donor level at E_c −0.145 eV and the acceptor level below the valence band edge at E_V −0.085 eV. These level positions define $\varepsilon(\pm)$ well above the valence band edge at around E_v +0.2 eV and make Mu an amphoteric impurity in Ge [36, 37]. The results are supported by the trend of Mu levels in SiGe alloys [38] and the pinning behavior of the universal alignment of the Mu occupancy level in different semiconductor hosts [39]. Figure 2.2 depicts the measured Mu donor- and acceptor-levels in $Si_{1-x}Ge_x$ alloys. The shift of the conduction and valence bands follows the calculated band offset. The position of the occupancy-level Mu[±] was determined from the experimental donor and acceptor data [38].

Although the μSR results support the general theoretical picture of hydrogen in semiconductors, the $\varepsilon(\pm)$ position of the Mu is higher in energy compared to the value for hydrogen calculated in Ref. [30]. Whether the 0.2–0.5 eV difference (depending on the published values) is due to the non-equilibrium conditions of the μSR experiment [31] or indicates that the calculated values should be corrected [38] remains an open question.

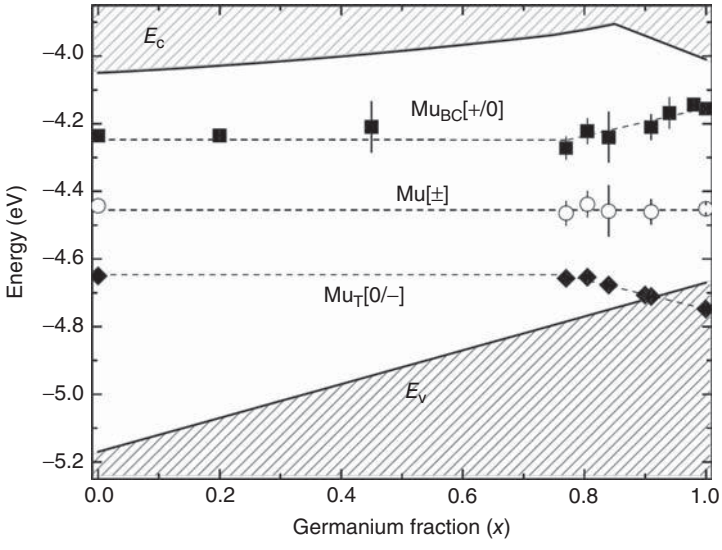

Figure 2.2 Band-alignment diagram of the Mu donor- and acceptor-levels in $Si_{1-x}Ge_x$ alloys. The occupancy-level Mu[±] was determined from the experimental donor and acceptor energies. From Ref. [38].

Low-temperature proton implantation stabilizes the metastable states of interstitial hydrogen and allows to study not only the level positions but also the LVMs of differently bonded hydrogen states. In Ge, a stretch vibration of $H_{BC}{}^{+}$ at 1794 cm^{-1} (Si 1998 cm^{-1}) and a degenerate mode at 745 cm^{-1} due to H^{-} close to the T-site could be identified [24]. There is no comparable LVM for hydrogen at the T-site in Si. DLTS measurements determined the position of the BC donor level at E_C −0.110 eV but failed to detect the acceptor level in p-type material [25].

2.2.3 Hydrogen Dimers

2.2.3.1 Interstitial H_2

Hydrogen molecules were proposed first to explain the reduced diffusivity of hydrogen in ultra-pure Ge [18]. Theory suggested stable molecular hydrogen on interstitial sites in crystalline Si [40, 41]. A study on Ge gave qualitatively similar results [42]. Several experimental studies verified molecular hydrogen in Si [43–51], Ge [52], GaAs [53, 54], and ZnO [55]. In all hosts, H_2 behaves as a freely rotating molecule at interstitial T-sites (Figure 2.3).

Figure 2.4 provides Raman spectra of a Ge sample after exposure to a pure hydrogen, pure deuterium, and a mixed H/D (1 : 1) plasma [52]. Best intensities were achieved in p-type samples which were treated in the plasma at ∼150 °C. A doublet with two sharp Raman components at 3826 and 3834 cm^{-1} was detected in the hydrogen-plasma treated sample. The deuterium plasma produces a line at 2782 cm^{-1}. This frequency is approximately a factor of $\sqrt{2}$ smaller compared to the hydrogen lines, indicating that hydrogen is involved in the vibration.

In analogy to the studies in Si, the lines at 3826 and 3834 cm^{-1} are assigned to ortho (nuclear spin 1) and para (nuclear spin 0) interstitial H_2 trapped at the T-site within the Ge host lattice. For ortho (para) H_2, the lowest possible value for the rotational quantum number is $J = 1$ ($J = 0$) due to the requirement of an antisymmetric total wavefunction. The detected intensity ratio of approximately 3 : 1 for the two lines as well as the 8 cm^{-1} line splitting strongly support this assignment.

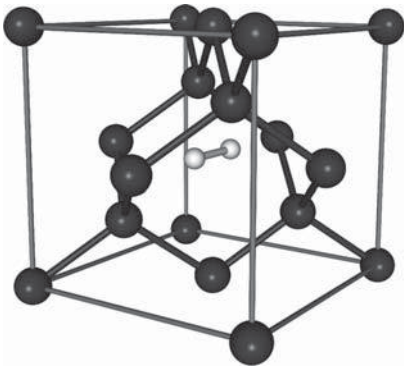

Figure 2.3 Position of the freely rotating H_2-molecule on the interstitial T-site in the diamond lattice.

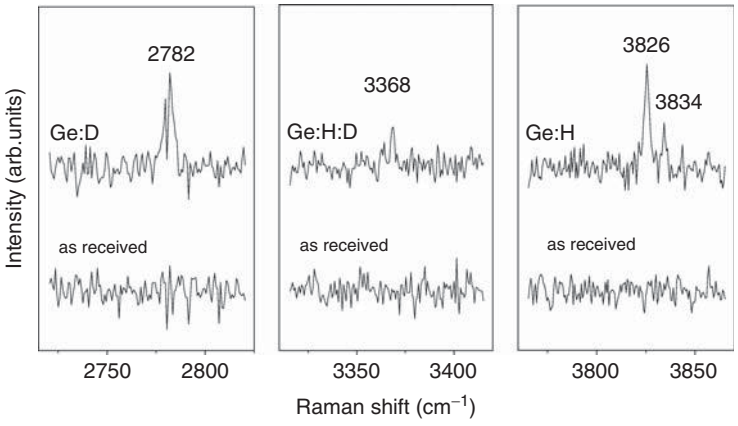

Figure 2.4 Raman spectra of interstitial H_2-molecules in Ge and the corresponding reference spectra of the as-received sample. The p-type (100)-Ge sample was exposed for 8 h at 175 °C to a D-, H:D(50 : 50)-, or H-plasma. The temperature within the laser excitation area was approximately 80 K. Integration time was 30 h. Adapted from Ref. [52].

For D_2, only one line is visible (the splitting seen in Figure 2.4 is due to an artifact of the CCD detector). The expected ortho-para splitting of D_2 is 2.5 cm^{-1}, which is well below the resolution limit of the monochromator.

No clear Raman signal from the HD-molecules could be observed in the samples when using a mixed H : D plasma. From the observed frequencies for H_2 and D_2, the expected LVM of the HD-molecule can be estimated to be at ~3360 cm^{-1} [48]. With some imagination there might be an indication for a signal at 3368 cm^{-1} in the spectrum of the sample after exposure to an H : D plasma, but the signal is too weak for a definite assignment. Possible explanations why the HD-line is not visible are provided in Ref. [52]. *Ab initio* calculations for interstitial H_2 in Ge and other hosts support the identification of the Raman lines [42, 52].

The low intensity of the H_2 Raman signal in Ge compared to that in Si can be attributed to the much smaller penetration depth of the laser and a lower efficiency of incorporating hydrogen during the plasma process [22].

2.2.3.2 The H_2^* Defect

The H_2^* defect, another hydrogen-dimer is shown in Figure 2.5. This dominant defect in proton-implanted Si binds one hydrogen atom close to a BC-site and the other one along the same trigonal axis at an AB site [56]. Theory predicts that the relative stability of interstitial H_2 as compared to H_2^* grows with the host lattice constant for the group IV elements. In Ge, interstitial H_2 is expected to be the ground state of hydrogen [57, 58]. Ge samples after low-temperature proton implantation reveal several absorption lines (two stretch modes at 1774 and 1989 cm^{-1}, a bend mode at 765 cm^{-1} and its first overtone at 1499 cm^{-1}), which were identified with the LVMs of the H_2^* complex [59]. The H_2^* defect in Ge anneals out at 145 °C compared to 200 °C for the same defect in Si.

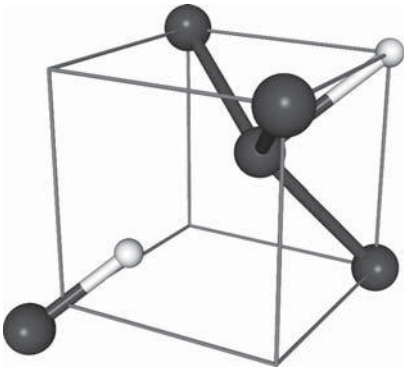

Figure 2.5 H_2^* defect with one hydrogen atom close to a BC-site and the other one along the same trigonal axis at an AB site. Adapted from Ref. [56].

Irradiation of Si by electrons, γ-rays, and neutrons transfers quenched-in "hidden" H_2-molecules into the H_2^* defect [60]. The transfer process involves the participation of vacancies and/or self-interstitials, although the exact details of the process are controversially discussed [60–62]. In Ge, similar studies with γ-rays allowed to determine the amount of hidden hydrogen in ultra-pure Ge [14].

2.2.3.3 H_2 Molecules in Hydrogen-Induced Platelets

High concentrations of hydrogen introduced by implantation in several semiconductors led to the formation of extended planar defects. In 1995, this phenomenon was first used for the formation of thin crystalline films on insulators (SOI) [63]. The so-called Smart-cut® technique involves bonding the implanted donor wafer surface onto an oxidized Si wafer or other substrates. A thermal treatment leads to the cracking of the donor wafer at the implantation depth of the ions and to an SOI structure on top of the substrate [64].

Hydrogen plasma treatment of Si and Ge samples under remote conditions generates well-defined platelets on (111) lattice planes ({111}-platelets) [65]. The platelets are stabilized by atomic hydrogen. In Ge, two broad Raman bands at ~1980 and ~4155 cm^{-1} are detected after exposure to the hydrogen plasma (see Figure 2.6) [66]. The former is close to the expected frequency of the stretch LVM of Ge–H, [59] the latter is close to the stretch mode of free H_2-molecules [67]. The two bands shift downward in energy by a factor of $\sim \sqrt{2}$ to 1430 and 2990 cm^{-1} when hydrogen is replaced by deuterium. Exposure of the Ge sample to a mixed H:D plasma adds an additional band at 3625 cm^{-1}. The band proves that the signal at 4155 cm^{-1} originates from a molecular hydrogen complex. As in Si, the H_2-molecule is trapped in larger voids or platelets, which provide stretch frequencies close to those of free H_2 [45]. The polarization dependence of the Raman signals points to a trigonal symmetry of the Ge–H bond and a freely rotating H_2-molecule within {111}-platelets (for details, see [66]). The behavior of the Raman bands is very similar to the results in Si where due to larger intensities, a more detailed polarization study was possible [68].

Information about the platelet formation process comes from intensity changes of the Ge–H and H_2-bands with sample temperature T_{plasma} during plasma

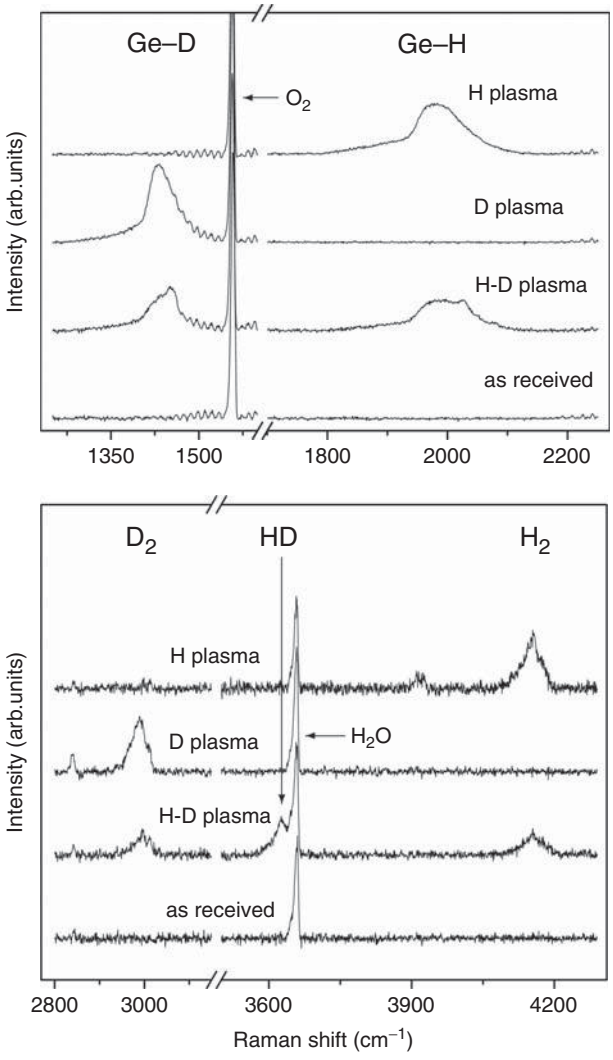

Figure 2.6 Room temperature Raman spectra of a Ge sample after exposure for 16 h at 150 °C to an H-, D-, and H:D-plasma (50 : 50) along with the reference spectra of the as-received sample. Integration time was 20 min for the spectral region 1250–2250 cm^{-1} and 140 min for the spectral region 2800–4290 cm^{-1}. The strong H_2O Raman line originates from water vapor along the optical path of the set up. Figure adapted from Ref. [66].

treatment (Figure 2.7). The Ge–H related signal is strongest at RT and decreases with increasing temperature. Above ~125 °C the signal from Ge–H is constant and disappears above 250 °C. The H_2 signal reaches the maximum intensity at around 125 °C and disappears with the Ge–H signal. Similarly to the platelet formation process in Si an agglomeration of H_2^* defects at low temperatures leads

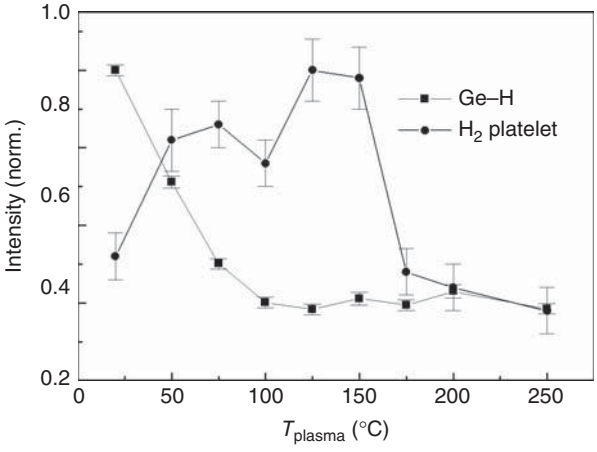

Figure 2.7 Dependence of the integrated and normalized intensities of the Raman bands at 1980 cm^{-1} for Ge–H and 4155 cm^{-1} for H_2 on sample temperature T_{plasma} during plasma treatment. From Ref. [66].

to an extended platelet structure $[H_2^*]_n^D$, as was suggested in Ref. [69] for Si and in Ref. [70] for Ge. At temperatures around 125 °C a restructuring of the defects occurs and an open structure which contains H_2-molecules $[2Ge–H + H_2]_n$ is formed. The increasing H_2-pressure inside the platelets causes the well known blistering and defoliation. This mechanism of a hydrogen-induced platelet formation needs no nucleation sites. A high hydrogen (H_2^*) concentration was found to be enough to induce platelet formation [71]. The creation of H_2^* in Si is favored if the Fermi level position at the plasma treatment temperature is close to the hydrogen occupancy level $\varepsilon(\pm)$ [72].

Proton implantation used in the original Smart-cut® process leads to a somewhat more complicated defect formation process. Implantation produces different hydrogen defects which were identified by FTIR spectroscopy [73]. Upon annealing, some of these structures are lost and the hydrogen therein is free to move to more stable configurations such as larger V_2H_6 or V_nH_{n+4} clusters which act as the nucleation points for internal cavities like {100}- and {111}-platelets. Upon further heating, molecular hydrogen will be trapped in these cavities, and the pressure on the internal surfaces causes cracks to extend and coalesce [74, 75]. From FTIR measurements larger vacancy clusters (e.g., V_2H_6 and V_nH_{n+4}) appear to be the key building blocks of the platelets.

2.2.3.4 Complexes of Hydrogen with Other Defects

Most of the hydrogen which is incorporated in Ge is electrically inactive in the form of dimers or impurity complexes. By γ-irradiation or rapid quench from higher temperatures to RT the inactive hydrogen activates isoelectronic substitutional C, Si, or interstitial O, and generates unwanted shallow acceptors A(H,C)

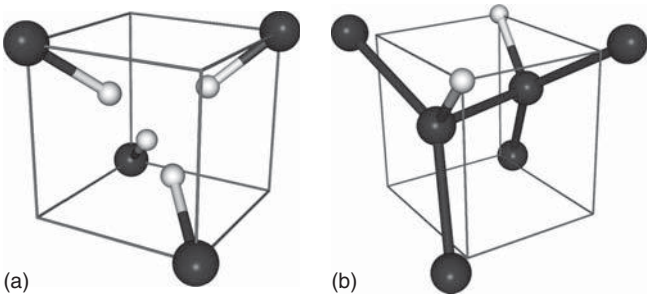

Figure 2.8 Proposed structures for the VH_4 (a) and IH_2 (b) complexes. Adapted from Refs [26, 81].

and A(H,Si) or shallow donors D(H,O) in ultra-pure Ge [11, 76]. The detailed electronic structure of the complexes could be revealed by the PTIS technique even at defect concentrations below 10^{11} cm^{-3} [77].

Acceptor-like behavior is also observed for the single level shallow-acceptor complexes A(Be,H), A(Zn,H), and A(Cu,H_2) [78]. Some of the hydrogen-induced centers exhibit a trigonal structure. Others seem to exhibit a peculiar tunneling of the hydrogen atom [79, 80].

Intrinsic defects like vacancies, self-interstitials, or their complexes can saturate their dangling bonds by hydrogen. Several defects involving Ge-vacancies or self-interstitials (V_nH_m, IH_n) were identified by LVM spectroscopy [27, 81]. Figure 2.8 provides examples for two possible defect structures, the vacancy with four hydrogen atoms (VH_4) or the self-interstitial with two bonded hydrogen atoms (IH_2). Part of the defects are electrically active, for example, VH has an acceptor level at E_V +80 meV, that affects the conductivity of dislocation-free, ultrapure Ge but is passive after trapping another hydrogen atom to form VH_2 [82].

Hydrogen passivation of deep impurity levels in Ge helped to produce ultrapure Ge. Hydrogen leads not only to a total passivation of deep donor and acceptor states of TMs in Ge but also to the formation of new electrically active TM–H complexes [21, 23, 83]. Copper forms with one or two hydrogen atoms complexes, which were identified by PTIS and Hall measurements [84, 85]. DLTS confirmed the earlier results [86–89]. A neutral Cu–H_3 complex was proposed based on a simple suggestive model where three hydrogen atoms can replace the three holes in the triple acceptor. A very similar behavior was derived in Si from DLTS profiling of Cu defects [90]. Again the defects Cu–H and Cu–H_2 are electrically active and the inactive species is associated with the Cu–H_3 complex.

In view of the results on different TM hydrogen complexes in Si, the early reports on the total passivation of such deep defects in Ge have to be checked carefully. Recent DLTS work on Co doped p-type Ge showed a total passivation of Co up to 6 µm, but deeper in the sample hydrogen related complexes could be observed (see Figure 2.9) [91]. Some recent reports support a very similar complex formation of hydrogen and TMs in Ge and Si [92].

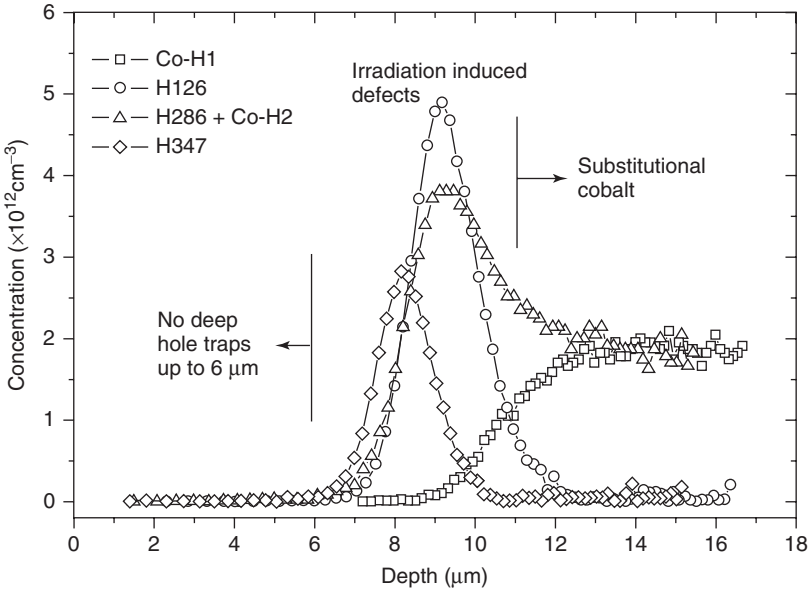

Figure 2.9 DLTS depth profile of defects in Co implanted Ge after hydrogen plasma treatment. H126, H286, and H347 refer to levels generated by the plasma damage. Co–H1 corresponds to cobalt hydrogen complex. From Ref. [91].

2.3 Hydrogen Passivation of Shallow Donors and Acceptors in Ge

The passivation of the electrically active shallow dopants by hydrogen is a well-understood phenomenon in Si and several other semiconductors. Until recently, however, the situation in Ge was controversial and clear direct evidence of passivation was missing.

In ultra-pure Ge crystals the radial dopant distribution showed a p–n junction for wafers close to the tail of the boule, with an inner n-type area and an outer p-type region. This "coring" could be removed by annealing at temperatures, which did not remove all the hydrogen from the wafer. Passivation of the residual acceptors Al or B by hydrogen was suggested but not directly verified [12, 13]. In the effusion study of hydrogen from plasma-treated p-type Ge, the authors mention the difficulty of passivating dopants in Ge by plasma treatments around 200 °C [22]. From the reflection close to the free carrier plasma edge the authors were not able to observe acceptor passivation for samples at temperatures in the range from −30 to 200 °C. Evidence for an interaction of H with In-acceptors in Ge was presented by $\gamma-\gamma$ Perturbed Angular Correlation measurements. The identification was based on the identical quadrupole interaction frequencies of the In-H pair in Si [93]. The only direct evidence for acceptor passivation in Ge is reported in Refs [1, 94]. In a figure the deactivation of the B–H complexes in Si, Ge, and the donor–hydrogen (DH) complex in Si doped GaAs is presented. The B–H

pairs are less stable in Ge than in Si. In Ge, the pairs are completely dissociated already at 100 °C, while some complexes still exist in Si at 180 °C. The Ge sample in this study was a boron-implanted n-type Ge, which was treated in a H-plasma at ∼50 °C. The passivation was detected in this study by Hall measurements.

Theory predicts for Ge similar to Si stable neutral complexes of the shallow boron acceptors with hydrogen [95, 96]. No calculation exists about passive shallow DH complexes in Ge.

2.3.1 Donor Passivation

In our studies on Ge we could recently establish the passivation of P- and Sb-donors by hydrogen [97, 98]. Hydrogenation of the samples was performed in a remote dc-hydrogen plasma in the temperature range from 40 to 150 °C for 2 h. The detection of the donor passivation was achieved by *CV*-measurements on Schottky diodes. Net carrier profiles were calculated from the capacitance according to the standard procedure provided in Ref. [99].

The passivation of the donors close to the surface reduces the donor concentrations from 10^{15} down to 10^{14} cm^{-3}. A higher temperature of the sample in the plasma introduces more hydrogen into the sample but also increases the dissociation of the DH pairs. A significant part of the shallow donors (about 20%) was neutralized up to about 4–5 μm below the junction in the sample treated at 150 °C.

The evolution of the carrier profiles was studied after annealing the Schottky diodes under (reverse bias annealing RBA). In the RBA experiments the sample was heated with the reverse bias-on from 200 K to the annealing temperature. After annealing for some time the sample was quenched to 200 K still with reverse bias applied. At that temperature the *CV*-profiles were recorded.

Figure 2.10 shows the results of a hydrogenation at 40 °C and subsequent RBA at 380 K for a P-doped Ge sample. The active donor concentration is reduced from 8×10^{14} to $\sim 1 \times 10^{14}$ cm^{-3} in the first 1.5 μm below the contact. The effect of the subsequent annealing results in changes in the active donor distribution. The P-donors are reactivated in the high-field region of the depletion layer due to the dissociation of the PH complexes. The high electric field sweeps the H species toward the bulk where the electric field is significantly reduced. Under reverse bias (−10 V) the electric field is directed toward the semiconductor and negative mobile species drift toward the bulk. The results of the RBA are consistent with a negative charge state of H in n-type Ge.

The thermally released H from the DH pair drifts from the high-field region into the bulk under reverse bias. In the low field region retrapping occurs and new dopant–hydrogen complexes form. Within 10% experimental error we find identical concentrations for released and trapped hydrogen after each annealing step for annealing times below 30 min.

The dissociation process for a DH pair

$$DH \leftrightarrow D^+ + H^-$$

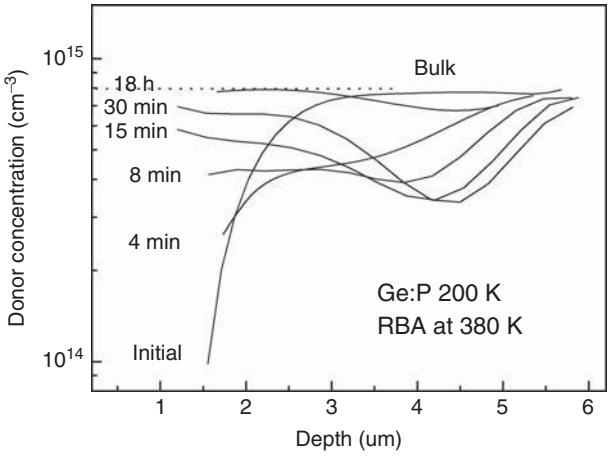

Figure 2.10 Depth profiles of the shallow P-dopant concentration in n-type Ge after a dc H plasma treatment at 40 °C during 2 h and subsequent reverse bias anneal ($V_R = -6$ V) at 380 K. The *CV*-curves were recorded at 200 K. Adapted from Ref. [98].

can be described as follows:

$$\frac{\partial[\mathrm{DH}]}{\partial t} = 4\pi R_B D_H [N_{D0} - [\mathrm{DH}]][\mathrm{H}] - \nu_{DH}[\mathrm{DH}] \tag{2.1}$$

[H] and [DH] are the concentrations of free atomic hydrogen and DH complexes, respectively. N_{D0} is the initial donor concentration. D_H is the diffusity of atomic hydrogen. R_B is the capture radius and ν_D the dissociation frequency of the DH complex. For simplicity the formation of H_2-molecules is neglected and all hydrogen ions are in one charge state.

In the high- field region of the Schottky contact the retrapping of H is low and the drift term ν_{DH} [DH] in Eq. (2.1) dominates. This leads to the experimentally observed first order dissociation. The dissociation energy can be easily calculated from the time dependence of the reactivation process close to the surface.

$$N_D - N(x,t) = C \exp(-\nu_{DH}(T)t)$$
$$\text{with } \nu_{DH}(T) = \nu_0 \exp(\Delta S_{Diss}/k - \Delta H_{Diss}/kT) \tag{2.2}$$

where ν_0 is the attempt frequency, ΔS_{Diss} the entropy of the dissociation process, and ΔH_{Diss} is the enthalpy of the dissociation process.

The analysis of the thermal stability of the dopant–hydrogen complexes is usually disturbed by retrapping of the thermally released hydrogen in the high-field region. An experimental control for a negligible retrapping is the bias independence of the dissociation energy [100, 101]. The retrapping of H, if overlooked, leads to the apparent increase of the dissociation enthalpies.

Figure 2.11 shows the annealing characteristics of the PH complexes in the high-field region at 1.5 µm for RBA anneals at different temperatures. The decrease of the PH concentration follows first order kinetics. The corresponding dissociation

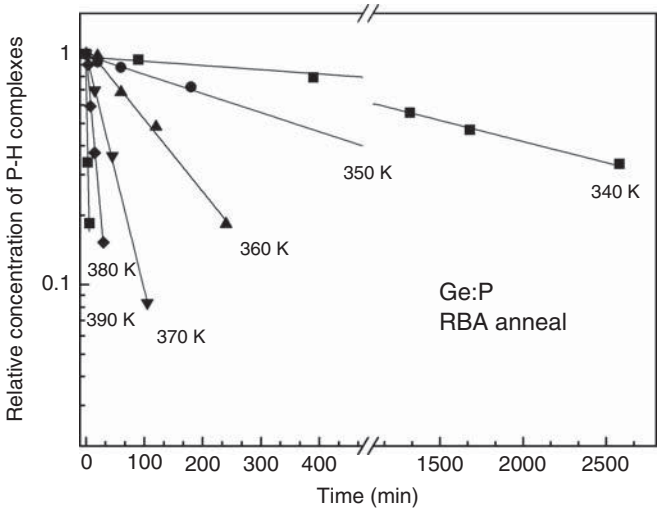

Figure 2.11 Concentration of inactive PH-pairs with annealing time under reverse bias. Concentration was determined from the *CV*-profiles at 1.5 μm below the contacts (same sample as in Figure 2.10). From Ref. [98].

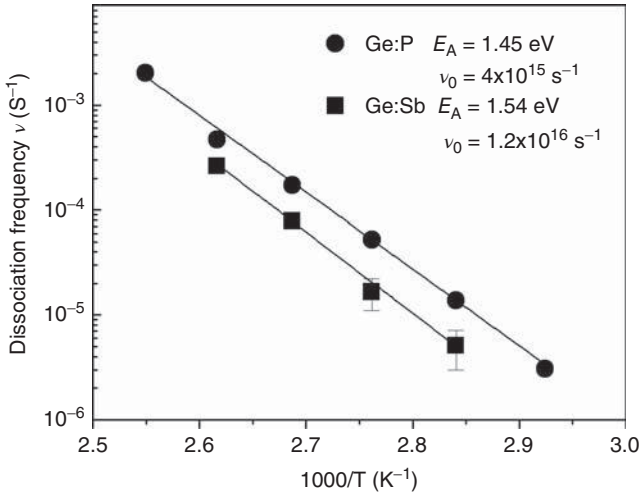

Figure 2.12 Arrhenius plots for the dissociation of PH and SbH pairs in Ge. The solid lines represent fits to the experimental data according to Eq. (2.2). From Ref. [98].

frequencies $\nu_{DH}(T)$ at different RBA temperatures are provided in the Arrhenius plot in Figure 2.12.

The enthalpy of the PH dissociation is according to Eq. (2.2) 1.45 ± 0.03 and 1.54 ± 0.2 eV for the SbH complex. Taking into account that the migration enthalpy of the H atom should be between 0.4 and 0.5 eV [16, 25] one can estimate a 1 eV binding enthalpy of the PH and SbH complexes. The pre-exponential factor

$\nu_0 \exp(\Delta S_{Diss}/k)$ was found to be about 5×10^{15} and $1 \times 10^{15}\,s^{-1}$ for the PH and SbH complex, respectively. The attempt frequency ν_0 is expected of the order of a typical phonon frequency in the lattice. In Ge, the frequency of optical phonons at 300 K is approximately $9 \times 10^{12}\,s^{-1}$. The high pre-exponential factor indicates strong entropy changes of $6-7\,k_B$ during the dissociation process. The origin of the entropy changes could be related to charge state changes or strong vibronic contributions to the dissociation process. The result in Ge is in variance with the observations of the attempt frequencies of the DH and acceptor–hydrogen defects in Si and GaAs where the entropy term could be neglected.

Compared to the P-doped sample the Sb doped sample showed a dependence of the dissociation enthalpy on the bias voltage. This behavior of the SbH dissociation was discussed already in Ref. [97]. A different technique to study the dissociation process directly was proposed. During RBA the capacitance of the Schottky contact decreases, due to the redistribution of ions inside the depletion layer. At longer anneals the capacitance increases again due to the hydrogen out-diffusion of the space-charge-region (SCR). From the initial decrease the dissociation energy of the pair can be derived. This method of directly recording the transient during RBA allows measurements on a shorter timescale, which is advantageous in n-type Ge or other semiconductors, when strong retrapping of the dissociated hydrogen occurs. In Ref. [97] a dissociation enthalpy of 1.36 ± 0.06 eV for the SbH complex in Ge was detected, which seems to be more reliable than the above value of 1.54 ± 0.2 eV.

2.3.2
Hydrogen in p-type Ge

The many negative reports about the difficulties to fabricate Schottky contacts on this material first discouraged us to study the influence of hydrogen on p-type Ge samples. In our investigation we used several p-type Ge samples with different dopants and dopant concentrations [29]. Astonishingly, good Schottky contacts could be fabricated on one sample. The Cz-grown, polished, Ga-doped sample had a doping concentration of around $2 \times 10^{15}\,cm^{-3}$ as determined by Hall measurements. Schottky contacts were formed by vacuum evaporation of Al through a mask onto the polished site of the samples. No cleaning step was used prior to the metal evaporation. For ohmic contact formation a eutectic InGa alloy was rubbed onto the rear side of the samples.

Figure 2.13 shows the RT IV-characteristic of the Schottky diode (as-received). The rectifying ratio $r = I(V)/I(-V)$ at ± 1 V amounts to 290 and the reverse leakage current at -2 V is $1.2 \times 10^{-2}\,A\,cm^{-2}$. The carrier concentration shown in Figure 2.14a of the as-received sample is determined by CV-profiling by changing the reverse voltage from -4 to 0 V. The 0 V position corresponds to the intrinsic SCR of the sample. The sample was cooled down from RT to 40 K without applied reverse bias. The profile is flat in the bulk and corresponds to the acceptor concentration. Only close to the surface an increase in negative charge is detected. CV-measurements at increased temperatures show below 150 K

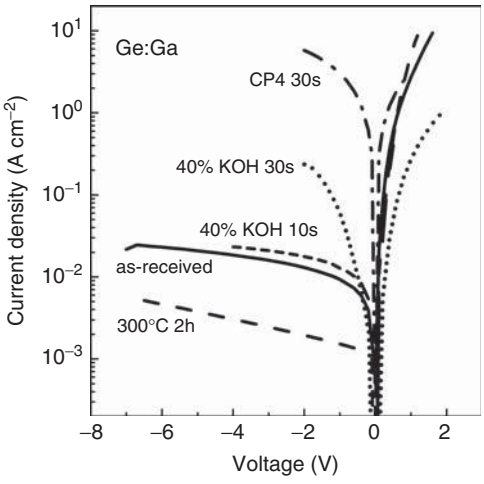

Figure 2.13 Room-temperature *IV*-curves of Al-Schottky diodes. The as-received Ga-doped Ge sample was annealed at 300 °C for 2 h, dipped in KOH for 10 and 30 s, or etched for 5 s in CP4 before Al evaporation. Schottky behavior is only observed for the as-received sample, the 300 °C annealed sample and the sample etched in KOH for 10 s. All other samples exhibit ohmic behavior. Adapted from Refs. [29].

profiles identical to the one at 40 K. However, when the temperature reaches 150 K we observed a stronger increase of the concentration close to the surface. A further increase in temperature results in profiles similar to the one shown in Figure 2.14a, which was recorded at 250 K (as-received (profile 250 K)). A reduction in the intrinsic SCR as well as an increase in negative charge close to the surface is visible. Apparently, a mobile negative species drifts during the *CV*-measurements toward the surface and increases the charge concentration in and close to the intrinsic SCR, which leads to the observed reduction in the SCR width. To reduce the concentration of mobile species in the sample we annealed the Ga-doped sample for 2 h at 300 °C in air. The *IV*-curve of the Schottky contact improved further, as is shown in Figure 2.13 (300 °C 2 h). The rectification ratio is now 3300, the reverse leakage current at −2 V is 1.9×10^{-3} A cm^{-2}. Annealing in pure gases like N_2 or O_2 provides similar diode characteristics but different shunt resistances.

The carrier profile of the annealed sample is shown in Figure 2.14b. Again the carrier profile is flat in the bulk and increases close to the surface. The increase at 250 K is less compared to the as-received sample and the reduction in the width of the intrinsic SCR is negligible. Apparently, less mobile negative charges exist in the annealed sample.

In the next step, we tried to incorporate hydrogen into the 300 °C annealed Ga-doped sample. Various different chemical treatments (HF, 40% KOH, 5% NaOH, and CP4 (hydrofluoric acid:nitric acid:acetic acid (3 : 5 : 3))), all known from Si to incorporate H, were applied. In addition, we treated the samples in dc-hydrogen plasma at sample temperatures in the range of 70 – 250 °C for 2 h.

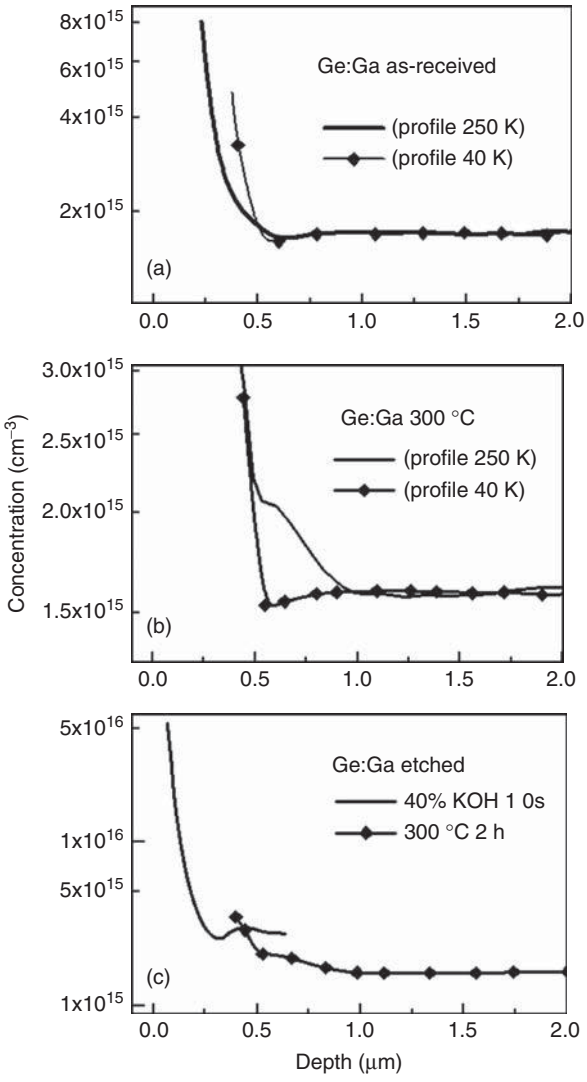

Figure 2.14 CV-profiles of Ga-doped Ge: (a) as-received sample, profiles measured at 40 and 250 K, (b) annealed sample, profiles measured at 40 and 250 K, and (c) etched sample compared to annealed sample, profiles measured at 250 K. Data from Refs. [29].

The KOH dip of 10 s leads already to a degradation of the Schottky diodes. The leakage current becomes larger, whereas the rectification ratio becomes smaller compared to the as-grown sample (see Figure 2.13 (40% KOH 10 s). Ohmic behavior is found after KOH etching for 30 s and CP4 etching (see Figure 2.13). Treatment in HF (40%, 5 s), NaOH (5%, 30 s), or in hydrogen plasma gave only ohmic behavior in all cases.

Figure 2.14c shows the carrier profile of the sample etched in KOH for 10 s. In addition to the flat profile of the annealed sample a strong increase of the negative charge close to the surface and a reduction of the intrinsic SCR is detected. Close to the surface the negative charge is more than a factor 5 above the acceptor doping concentration; this increase explains the leakage current increase in this sample (see Figure 2.13).

Our results provide strong evidence that the presence of hydrogen hinders the Schottky barrier formation in as-grown p-type Ge samples. Under our experimental conditions hydrogen should be mobile and negatively charged at RT. The ionized shallow acceptors will drive H^- toward the surface, which acts as a sink for defects in many semiconductors. This increase in the concentration of the mobile defects toward the surface is clearly observed in the CV-profiles (see e.g. the KOH treated sample in Figure 2.14c). H^- adds to the negative surface charge and leads to a significant reduction of the space charge layer width. Therefore, the absence of the Schottky barrier in the samples treated in the dc H-plasma or in wet chemical solutions can be explained by the presence of negatively charged H. Our study indicates a high hydrogen concentration of more than 10^{15} cm^{-3} even in the as-grown Ge samples. The existence of a Schottky barrier in the as-received Ga-doped sample and the ohmic behavior in our B- and Al-doped Ge samples indicate different hydrogen concentrations in the Ge samples.

Budde *et al.* [24] demonstrated that isolated H is mobile above 150 K. Cooling down the samples to 40 K without reverse bias applied leads to a freeze out of the H atoms in the crystal lattice. This immobilization of H is observed in our experiments (Figure 2.14a,b). The increase of the concentration close to the surface at 250 K is associated with the drift of mobile, negativelycharged hydrogen species. Further support for the detrimental effect of H on the formation of Schottky contacts in p-type Ge comes from the finding that all H-treatments (wet chemical etching and low-temperature H plasma treatments) lead to a degradation of the Schottky contacts.

The annealing of the samples at about 300 °C seems to be sufficient to significantly reduce the concentration of atomic hydrogen in the samples. The formation of H_2 molecules detected in Ref. [52] or an out diffusion of atomic hydrogen could be the origin of this behavior.

No passivation of negatively charged acceptors in the Ga doped samples after different H-treatments was observed in the present study. This is consistent with the assignment of H as a negatively charged defect which would not interact with negatively charged acceptors at around RT. This is also in agreement with the previous studies by Stutzmann *et al.* [22].

2.3.3
Schottky Contacts on p-type Ge

The annealing of the Ga doped sample at 300 °C for 2 h resulted in a significant improvement of the diode quality. This thermal treatment allowed us to form Schottky barriers also on our Al- and B-doped Ge samples. No rectifying contacts

were observed in these samples before the thermal treatment. The Schottky contacts on the Ga- and Al-doped samples exhibit at RT a reverse current density of about 10 mA cm^{-2} at −7 V. A similar quality of Schottky diodes on p-type Ge has never been reported before. In the annealed samples the barrier height determined from thermionic theory seems to be independent of the dopants (about 0.55 eV) (see Ref. [29]). The value is close to that reported in Ref. [102] for sulfur surface passivated samples.

Previously, the absence of Schottky barriers on p-type Ge was related to a pinning of the Fermi level to a charge neutrality level (CNL) or to surface states, which are located close to the valence band. In an experimental study Dimoulas *et al.* [103] suggested that the Fermi level was pinned to the CNL slightly above the valence band and as a result Schottky contacts were impossible to form at RT. The results were based on an estimate of the barrier heights in n-type Ge and their extrapolation for p-type Ge. One should also emphasize that the leakage current in the diodes of Ref. [103] was more than 2 mA cm^{-2} and reached even 200 mA cm^{-2} at −1 V for some of the diodes. The high leakage current indicates that the thermionic model cannot be used in Ge to determine proper barrier heights.

Rectifying junctions on p-type Ge were first achieved by In-plating or In evaporation [87, 88, 104]. The quality of the diodes at RT was however poor. Later, n^+p junctions were prepared by MBE (molecular beam epitaxy) growth [105]. After the MBE growth, the n^+p-structures had to be annealed at about 750 °C to improve the quality of the Sb doped n^+-top Ge layer. At these temperatures Sb diffuses into the p-type Ge substrate and deteriorates the electrical properties of the p-type layer. In another attempt Schottky diodes with up to 20 nm thin highly n-doped surface layers were created on p-type Ge by epitaxy, implantation, or diffusion [106]. However, the band bending of the highly doped n-layer did not lead to any improvement of the room-temperature *IV*-curves. Recently, Thathachary *et al.* [102] reported on the fabrication of Al and Zr Schottky contacts by sulfur passivation of the surface of p-type Ge. The barrier height for the metals was evaluated as 0.6 and 0.57 eV for Zr and Al, respectively, with a reverse bias current density of 10 mA cm^{-2} at −1 V for the Zr diode.

The properties of Ge surface states were reported by different groups [32, 33, 102, 107, 108]. A passivation of the Ge surface states was suggested in Ref. [109]. Hydrogen-terminated Ge (100) surfaces were achieved by wet chemical etching. Matsubara *et al.* [110] reported, however, only a small reduction of the interface state density after low-temperature hydrogen annealing.

The position of the Ge dangling bond states was calculated below the valence band edge in Refs [32, 33]. This leads to a negatively charged dangling bond state in p-type Ge. As mentioned above, interstitial hydrogen should also be negatively charged in p-type Ge and, therefore, a passivation of dangling bond states by hydrogen seems to be very ineffective in Ge.

Our experimental results ask for a critical review of the proposed Fermi level pinning in p-type Ge in view of the omnipresence of H in almost all Ge crystals. In contrast to earlier studies we were able to form Schottky diodes with low leakage currents (below 2×10^{-2} A cm^{-2}) in as-grown Ga-doped Ge even at RT. This

indicates that the Fermi level is not pinned in p-type Ge. However, we cannot exclude an additional influence of the surface states on the quality of Schottky contacts. More systematic studies are necessary to clarify the interaction of hydrogen with surface states in Ge.

2.4 Summary

Silicon and Germanium behave like "brother and sister" and exhibit in many respects very similar material properties [111]. This relationship is also reflected in the behavior of hydrogen in these materials. Early work on ultra-pure Ge revealed the formation of hydrogen complexes in low concentrations. Cooling the crystals from growth temperature quenched-in neutral, passivated complexes but also formed new electrically active defects. Later work on Si revealed very similar defects but also established the formation of passivated shallow acceptors and donors in high concentrations under equilibrium conditions. Owing to its high intrinsic carrier mobility Germanium has gained renewed interest as an active semiconductor material for advanced nanoelectronic devices. Progress has been made in the understanding of shallow level passivation, the behavior of interstitial hydrogen, H-dimers, and in the complexing of H with intrinsic or extrinsic defects in this material.

A general difference between Si and Ge seems to be related to the passivation of the crystal surface. Experimental results are needed to clarify the position of the dangling bond states at the Ge surface. There is also a need to determine by experiment the position of the occupation level $\varepsilon(\pm)$ in Ge directly. This would help to understand if acceptor passivation would be possible in highly doped p-type Ge samples.

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3
Epitaxy of Ge Layers on Blanket and Patterned Si(001) for Nanoelectronics and Optoelectronics

Jean-Michel Hartmann

3.1
General Introduction

With the increasing use of optical fibers in telecommunications, the demand for low-cost and efficient photo-detectors (PDs) operating in the low loss windows (1.3–1.6 μm) of silica fibers is growing rapidly [1]. Moreover, existing electrical interconnection technologies limit the performance of high speed computers and switching systems. An alternative, based on optical interconnections, is being studied. It requires the development of high speed (≥10 GHz), reliable, and compact optical terminal PDs compatible with the telecommunication wavelengths. Pure Ge grown directly onto Si(100) is the best candidate for such PDs, due to its band gap of 0.8 eV at room temperature [2–5]. Ge(001) layers can also be used in conjunction with advanced gate dielectrics such as HfO_2 for the formation of bulk Ge [6, 7] or Ge-On-Insulator (GeOI) [8–10]–based Metal Oxide Semiconductor Field Effect transistors (MOSFETs) with superior hole mobilities. Finally, due to their small lattice mismatch with GaAs ($a_{Ge} = 5.65785$ Å $\Leftrightarrow a_{GaAs} = 5.6533$ Å) and similar thermal expansion coefficients, Ge(001) layers are most interesting as templates for the growth of high quality GaAs-based heterostructures for diodes and solar cells [11], laser diodes [12], high electron mobility and heterojunction bipolar transistors (HEMTs and HBTs) [13, 14], III–V-On-Insulator substrates [15], and so on.

However, due to the large lattice mismatch with Si (4.2%), it is not easy to obtain on Si(001) Ge films with suitable characteristics, that is, a thickness which is high enough (i.e., >1 μm) for layer transfer and thus the elaboration of GeOI or SOLES (which stands for Silicon On Lattice-Engineered Substrate [14]) substrates, a flatness which is compatible with sub-micron lithography (and layer transfer), a minimum defect content for high speed devices (usually achieved for Ge layers thicker than 1 μm [6, 7]), and so on. Several routes have been explored during the last 15 years or so to obtain such films. SiGe virtual substrates (VSs) graded all the way up to pure Ge yield low threading dislocations densities (TDDs) ($\sim 10^6$ cm^{-2}), fully relaxed but rough (i.e., cross-hatched) Ge layers on top [16–18]. Chemical Mechanical Polishing (CMP) is then mandatory to recover smooth surfaces.

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Another one, which has been proposed initially by Colace *et al.* [19], followed quite closely by Hernandez *et al.* [20], relies on the deposition of a low-temperature Ge "seed" layer, followed by the deposition of a high temperature (HT) Ge layer [2, 19–26]. The Low Temperature (LT: 330–450 °C) adopted for the first Ge layer plastically relaxes the strain in the Ge film without any 3D islanding. The HT (600–850 °C) used for the growth of the second, topmost, Ge layer lowers the dislocation density and reduces the overall deposition time. HT thermal cycling under H_2 (in-between 750 and 875–900 °C, typically) can be called upon to further reduce the amount of defects in the layers (thanks to thermally assisted glide of the threading arms of misfit dislocations and mutual annihilation or elimination at wafer edges) [2, 23, 25–27]. Such a process is time-consuming, however, and induces significant Ge/Si intermixing at the interface [2, 25, 28].

We will present in the first part of this chapter the LT/HT growth and the structural properties of Ge thick layers on Si(001) substrates. We will then describe the Si passivation process that we use on nominal Ge(001) surfaces (prior to HfO_2/TiN/poly-Si gate stack deposition) in order to obtain high performance pMOSFETs on GeOI substrates. In a second part, we will present the challenges associated with the selective epitaxial growth (SEG) of pure Ge layers in Si cavities at the end of optical waveguides. In the third and final part, we will describe the approach we have used to fabricate compressively strained, high crystalline quality GeOI substrates (thanks to SiGe VSs) and present their structural and electrical properties.

3.2
Epitaxial Growth of Ge Thick Layers on Si(001)

3.2.1
Growth Protocol and Kinetics

The Ge layers were grown on slightly p-type doped 200 mm Si(001) substrates in an Epi Centura Reduced Pressure-Chemical Vapor Deposition (RP-CVD) industrial cluster tool. The flow of H_2 carrier gas was set at a fixed value of a few tens of standard liters per minute. Germane (GeH_4) diluted at 2% in H_2 was used as the source of Ge. The $F(GeH_4)/F(H_2)$ mass-flow ratio was equal to 7.917×10^{-4}. During growth, the wafer laid horizontally on top of a circular SiC-coated susceptor plate that rotated to improve the spatial thickness uniformity of the films. It was heated by two banks of 20 tungsten–halogen lamps (maximum power: 2 kW each) located above and below the susceptor assembly. Temperature monitoring and control was ensured through the lower pyrometer, that is, the one looking at the rearside of the susceptor plate on which the wafer laid.

Growth occurred in three steps. A Ge layer more than 100 nm thick was first grown at 400 °C, 100 Torr, that is, well above the temperature for which the Ge film would turn amorphous [21], in order to start from a rather flat, nearly fully relaxed Ge "seed" layer. In the second step, the temperature was ramped from 400 up to

750 °C (1 °C s^{-1}) and the growth pressure from 100 Torr down to 20 Torr while still having germane flowing into the growth chamber. Tens of nanometers of Ge were deposited during the second step. In the third step, a Ge layer with a thickness in-between 0 nm and more than 2000 nm was grown at 750 °C, 20 Torr in order to obtain the total desired thickness. The 400 °C, 100 Torr Ge growth rate was 8.6 nm min^{-1}, while the 750 °C, 20 Torr growth rate was 45.5 nm min^{-1}. Thermal Cycling (in-between 750 and 890 °C) was used afterwards to further reduce the amount of defects in the thickest layers. The number of cycles was 4 while the 750 and 890 °C annealing steps lasted 5 min.

3.2.2 Surface Morphology

We have grown various thickness Ge layers in order to have Atomic Force Microscopy (AFM) snapshots of the surface morphology at different stages of the LT/HT growth (and subsequent thermal cycling). 20 µm × 20 µm images

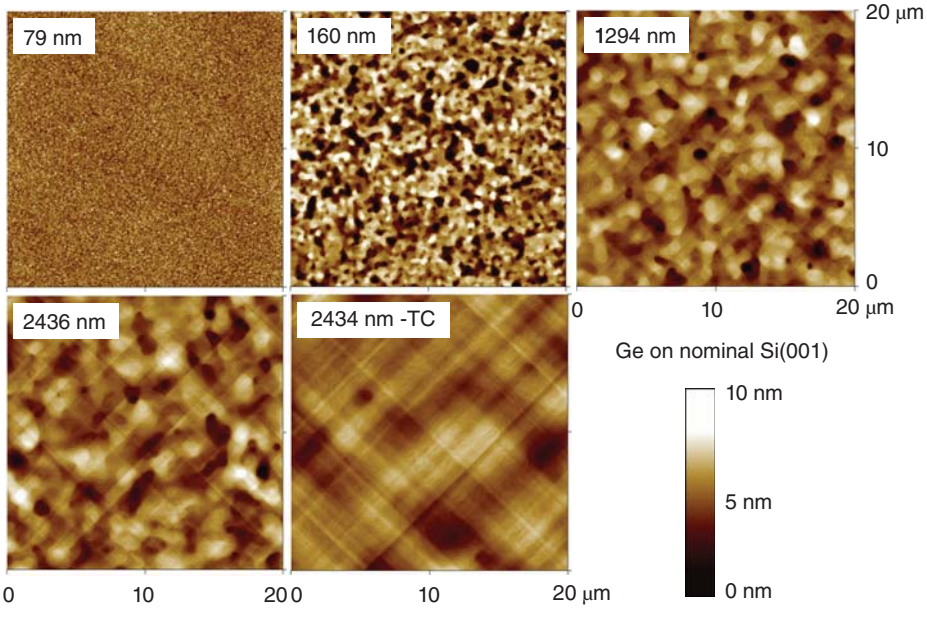

Figure 3.1 20 µm × 20 µm AFM images of the surface of various thickness Ge layers on Si(001). From top left to bottom right: a 79 nm thick Ge layer grown at 400 °C, a 79 nm thick Ge layer grown at 400 °C capped by 81 nm of Ge during the ramping-up to 750 °C (160 nm), a 160 nm thick Ge layer grown at 400 °C/750 °C capped by either 1134 nm of Ge or 2276 nm of Ge at 750 °C (1294 and 2436 nm images) and finally a 2434 nm thick Ge layer which has been submitted to a Thermal Cycling. Image sides are roughly along the <100> directions. From Ref. [26]. © IOP Publishing. Reproduced by permission of IOP Publishing. All rights reserved.

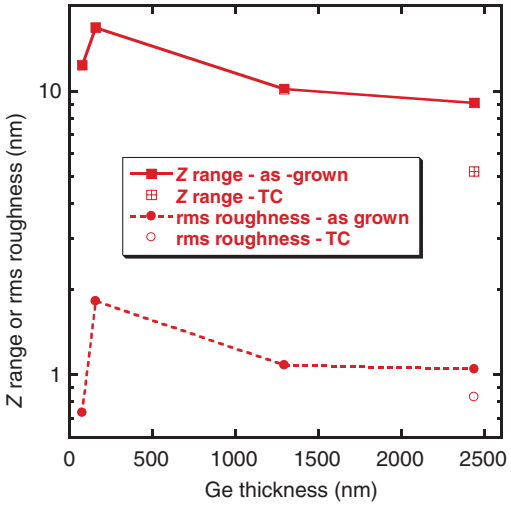

Figure 3.2 Root mean square surface roughness and *Z* range values as a function of the Ge layer thickness on nominal Si(001) substrates.

can be found in Figure 3.1. The surface is rather rough at 400 °C, with a huge number of randomly organized, very small spatial wavelength mounds. After the ramping (under GeH_4) from 400 up to 750 °C, the surface is not random anymore: numerous hills appear (several hundreds of nanometers at their base). During the thickening at 750 °C of the Ge layer, hills coalesce, becoming larger. Those hills are characterized by the presence on their sides on rather large terraces bordered by bi-atomic height steps. A regular array of undulations (or surface cross-hatch) along the <110> crystallographic directions is also quite obvious. It is due to the propagation of threading dislocations on {111} planes.

We have used those AFM images to quantify the evolution of the surface root mean square roughness (rms) and *Z* range ($= Z_{max} - Z_{min}$) of those Ge layers as a function of the deposited thickness (see Figure 3.2). The rms roughness and the Z range, which are around 0.7 and 11 nm for the 400 °C layers, increase to 1.6 and 15 nm just after the ramping-up to 750 °C. They then monotonously decrease as the Ge layer thickness grown at 750 °C increase, with 1.1 and 10 nm values for 2.4 µm thick layers. The thermal cycling actually smoothens the surfaces: rms and *Z* range values are indeed of the order of 0.8 and 6 nm only for annealed 2.4 µm thick Ge layers. Those surfaces are thus fit (after a capping with SiO_2) for a bonding thanks to the SmartCut™ process to oxidized Si substrates, this without any additional CMP step.

3.2.3 Strain State

We have used high resolution X-ray Diffraction (XRD) to quantify the macroscopic degree of strain relaxation $R = (a^{\parallel}_{Ge} - a_{Si})/(a_{Ge} - a_{Si})$ as a function of the

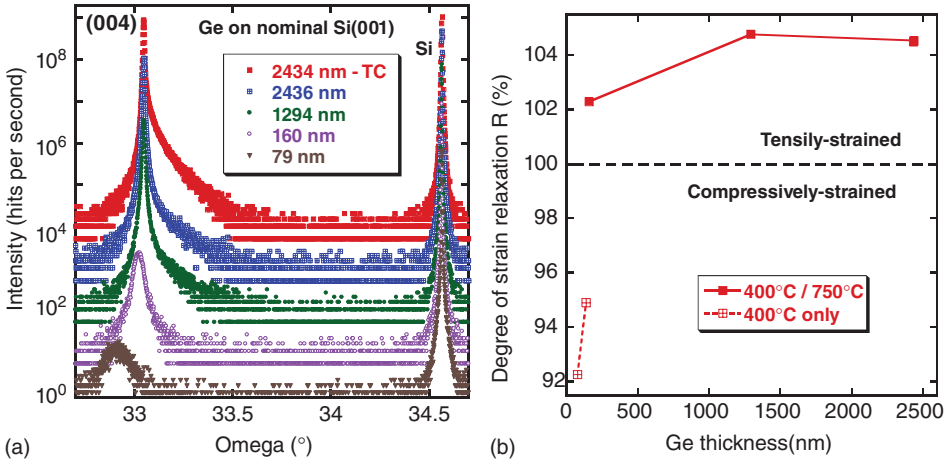

Figure 3.3 (a) Omega-2Theta scans around the (004) diffraction order for some of the Ge layers grown on Si(001). (b) Macroscopic degree of strain relaxation as a function of the Ge layer thickness on Si(001).

Ge layer thickness. $a_{Ge}^{\parallel}$, a_{Si}, and a_{Ge} are the in-plane lattice parameter of the Ge layer, the lattice parameter of the Si substrate (5.43105 Å) and the lattice parameter of bulk Ge (5.65785 Å), respectively. We have plotted in Figure 3.3a typical XRD profiles around the (004) diffraction for various thickness Ge layers grown on Si(001). Apart from the Si substrate peak (located at 34.564°) we do have the presence at roughly 33° of the Ge layer peak, whose intensity drastically increases and full width at half maximum decreases as the Ge layer thickness increases. The asymmetry of the peak associated to the annealed 2.4 µm Ge layer is to be noticed: the high incidence angle component is indeed due to the interfacial GeSi alloy formed during the thermal cycling [2, 25, 28]. From the angular position ω_{Ge} of this peak, we can gain access to $a_{Ge}^{\perp}$, the lattice parameter of the Ge layer in the growth direction, thanks to the Bragg's Law : $2(a_{Ge}^{\perp}/4)\sin\omega_{Ge} = \lambda$, λ being the Cu $K\alpha_1$ wavelength (1.5406 Å). We can then determine R. $a_{Ge}^{\parallel}$, the in-plane lattice parameter of the Ge layer, is indeed deduced from $a_{Ge}^{\perp}$ thanks to the following formula: $a_{Ge} = \frac{1-\upsilon}{1+\upsilon}a_{Ge}^{\perp} + \frac{2\upsilon}{1+\upsilon}a_{Ge}^{\parallel}$, with $\nu = 0.271$. Setting aside the 400 °C Ge layers (which are still slightly compressively strained), all the Ge layers were found to be tensily strained ($R \sim 104\%$), see Figure 3.3b. This is due to differences in the thermal expansion coefficients between Ge and Si. The lattice parameter of Ge thick layers on Si substrates, which are almost fully relaxed at 750 °C (the growth temperature) or 890 °C (the upper temperature of the thermal cycling (TC)), shrinks differently from the one of a bulk Ge crystal. $a_{Ge}^{\perp}$ indeed shrinks with the thermal dilatation coefficients of Ge, whereas $a_{Ge}^{\parallel}$ shrinks with the smaller ones of the much thicker Si substrate underneath. We thus end up with tensily strained Ge layers [29].

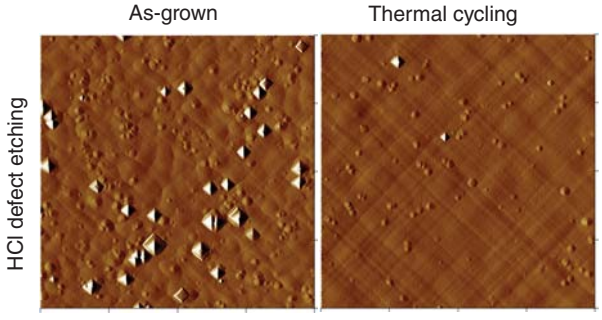

Figure 3.4 40 μm × 40 μm amplitude mode AFM images of the surface of as-grown and annealed 2.4 μm thick Ge layers on Si(001) after the HCl etching of roughly 190 nm of Ge. Image sides are roughly along the <100> directions. From Ref. [26]. © IOP Publishing. Reproduced by permission of IOP Publishing. All rights reserved.

3.2.4
Defects Density and Distribution in the Ge Layers

We have also proceeded with *in situ* HCl decoration [30] of the threading dislocations present in the thickest Ge layers grown. Around 190 nm of Ge was etched at 450 °C. Numerous round and square-based etch pits shapes were obtained (see Figure 3.4). A clear impact of the thermal cycling on the TDD in 2.4 μm thick Ge layers was evidenced, with a reduction from $2 \pm 0.2 \times 10^7$ down to $7 \pm 0.1 \times 10^6\ cm^{-2}$ on nominal surfaces. We have otherwise used Secco wet etching, which is a quite powerful defect revelation technique [27], in order to have another TDD value for each sample. The same kind of TDD reduction upon annealing was evidenced on 2.4 μm Ge films: from $5 \pm 0.5 \times 10^7$ down to $1 \pm 0.1 \times 10^7\ cm^{-2}$.

Defect distribution in the film most likely explains the higher TDD obtained after Secco than HCl etching ($5 \Leftrightarrow 2 \times 10^7$ and $1.0 \Leftrightarrow 0.7 \times 10^7\ cm^{-2}$). We have plotted in Figure 3.5 cross-sectional Transmission Electron Microscopy (TEM) pictures of a 2.8 μm thick annealed Ge layer grown on a nominal Si(001) substrate. The 0.15 μm thick zone close to the Ge/Si interface has a dislocation density of the order of $10^{10}\ cm^{-2}$. The 1.3 μm Ge layer on top has a measured dislocation density around $1-2 \times 10^9\ cm^{-2}$. Finally, the topmost 1.35 μm thick Ge layer is characterized by a dislocation density of the order of $3-6 \times 10^7\ cm^{-2}$.[1)] Etching roughly 1.2 μm of Ge with Secco (in order to have etch pits which can be seen optically) instead of 0.2 μm with HCl brings us closer to the defected region, yielding higher TDDs.

An exponential decrease of the TDD with the Ge layer thickness has been demonstrated by several teams [25, 31, 32]. This has been put to good use by Yamamoto *et al.* in order to obtain superior crystalline quality Ge layers. They

1) The dislocation density ρ was calculated thanks to the following relationship : $\rho = L^{total}/(S \times t)$, where L^{total} is the sum of the lengths of all the dislocation lines visible in a zone, S is the zone area and t is the TEM lamella thickness in the zone (~0.3 μm in the bottommost 1.45 μm of the Ge layer and ~0.25 μm in the topmost 1.35 μm).

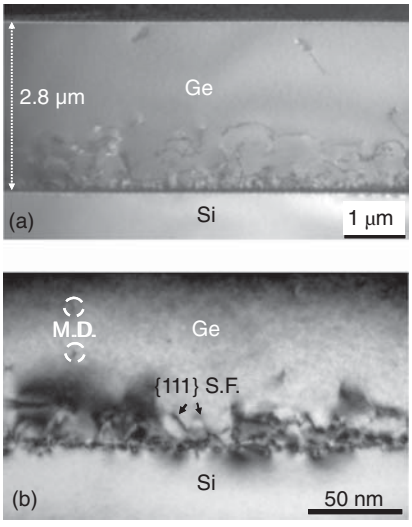

Figure 3.5 (a) Cross-sectional weak beam dark field TEM image of a 2.8 μm thick, annealed Ge layer grown on a nominal Si(001) substrate. (b) Dark field with close to Bragg conditions image (taken with $g = 220$) of the interface between Ge and Si. The {111} Stacking Faults (SF) observed in Figure 3.9b are the result of the dissociation of perfect Misfit Dislocations (MDs) into partial dislocations. From Ref. [26]. © IOP Publishing. Reproduced by permission of IOP Publishing. All rights reserved.

first grew 4.5 μm thick Ge layers on Si(001)and subsequently etched most of it *in situ* with gaseous HCl. Given that the TDD barely changed in the top 2.7 μm of their 4.5 μm thick Ge layers, they ended up with flat, ~1.8 μm thick Ge layers with a TDD barely above 10^6 cm^{-2} [32].

3.3 Ge Surface Passivation with Si

A major drawback in the use of Ge in advanced MOSFETs is the poor quality of its thermal oxide as compared to SiO_2. A Ge surface passivation prior to gate dielectric deposition is thus mandatory in order to obtain low interface state densities (D_{it}). Typical values in state-of-the-art Si-based devices are indeed below 10^{10} cm^{-2}.

By contrast, D_{it} values in Ge-based devices without surface passivation are typically 100–1000 times larger [33]. One of the solutions is to cap Ge with a very thin Si layer (at most 25 Å thick in order to avoid any plastic strain relaxation). As an illustration, we have plotted in Figure 3.6 a cross-sectional TEM image of the gate stack in one of our GeOI pMOSFETs [8]. Prior to the deposition of the HfO_2/TiN high-K/metal gate, we have passivated the Ge surface with 15 Å of Si (see below) then converted most of the thin Si layer into SiO_2 thanks to chemical oxidation.

3.3.1 Passivation Protocol

SiH_4 or Si_3H_8 are notably used as Si precursors for the growth at 500 or 350 °C of those thin Si cap layers, with 1.5×10^{11} cm^{-2} interface state densities only

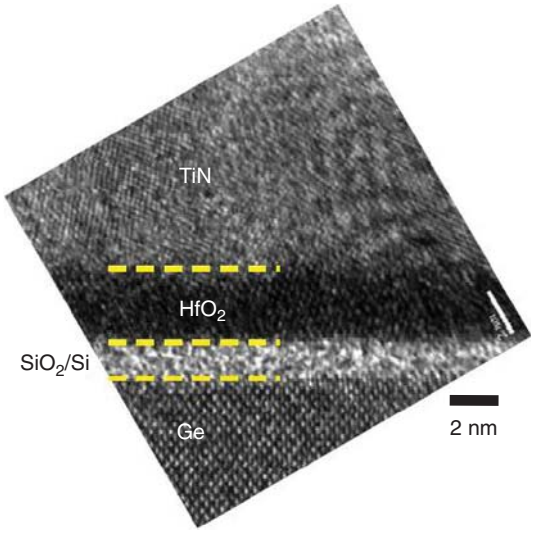

Figure 3.6 High resolution TEM image of a SiO_2/HfO_2/TiN/poly-Si gate stack on a GeOI substrate, the SiO_2 having been formed thanks to a Si surface passivation of Ge followed by a chemical oxidation step. From Ref. [26]. © IOP Publishing. Reproduced by permission of IOP Publishing. All rights reserved.

[34, 35]. We have proceeded here drastically differently. We have indeed adopted the approach pioneered by Lee *et al.* [36] and used by us roughly 10 years ago to cap with Si compressively strained Ge layers grown on $Si_{0.5}Ge_{0.5}$ VSs [37]. It consists in capping at LT the Ge surface with a few monolayers of Si prior to the actual deposition at higher temperature of the Si cap. This way, the surface roughening occurring during the temperature ramping-up is minimized.

After a "HF-last" wet cleaning and a 650 °C, 2 min H_2 bake, we have exposed at 550 °C, 20 Torr the nominal Ge(001) surfaces to SiH_2Cl_2, for 5 min. Growth occurred until the surface was covered almost exclusively by Si atoms then stopped. Indeed, Ge atoms present on the surface act at this temperature as H desorption sites. Slowing down but definite GeSi then SiGe growth rates are then achieved as we gradually get away from the pure Ge layer underneath (Si/Ge interdiffusion). Given that the homoepitaxy at 550 °C of Si with SiH_2Cl_2 is characterized by virtually nil growth rates [38], growth stops as soon as Ge atoms are not present on the surface anymore. The ~5 Å thick interfacial layer obtained after this step is most likely a graded SiGe alloy. We have then increased the growth temperature to 650 °C and sent SiH_2Cl_2 in order to benefit from roughly 5 Å min^{-1} homoepitaxial growth rates and thus tailor the Si cap layer thickness as desired. This two-step process is, because of the chlorinated gaseous precursor used, selective versus SiO_2, which is most useful on GeOI substrates with a mesa isolation scheme.

Switching, should the selectivity constraints be relaxed, from SiH_2Cl_2 to SiH_4 enables for the same mass-flow and growth pressure a 100 °C temperature

reduction both for the passivation step and the Si layer thickening (i.e., 450 °C/550 °C instead of 550 °C/650 °C). This is handy for thin, patterned GeOI substrates where moat recess and/or agglomeration might occur for high thermal budgets (by analogy with ultra-thin, patterned silicon-on-insulator (SOI) substrates [39]). This might also be useful for minimizing the diffusion of Ge into the Si cap during its thickening. A ~2 nm interface chemical width has indeed been evidenced when capping (at 350 °C/650 °C thanks to SiH_2Cl_2 [37]) with tensily strained Si a compressively strained Ge layer, itself on relaxed $Si_{0.5}Ge_{0.5}$ (Geometric Phase Analysis of cross-sectional high resolution TEM pictures) [40].

3.3.2
Surface and Film Morphology

We have imaged the surface of our thick Ge layers capped by 15, 20, or 25 Å of Si (using the passivation protocol described above). AFM micrographs can be found in Figure 3.7. For 15 Å of Si, hills with large terraces bordered by bi-atomic steps can be observed. They are however less well defined than for uncapped Ge layers.

For 20 Å of Si, numerous islands have nucleated on the terraces and a limited number of three-dimensional (3D) islands can also be observed (dots in the top right image). For 25 Å of Si, the surface is fully covered by numerous

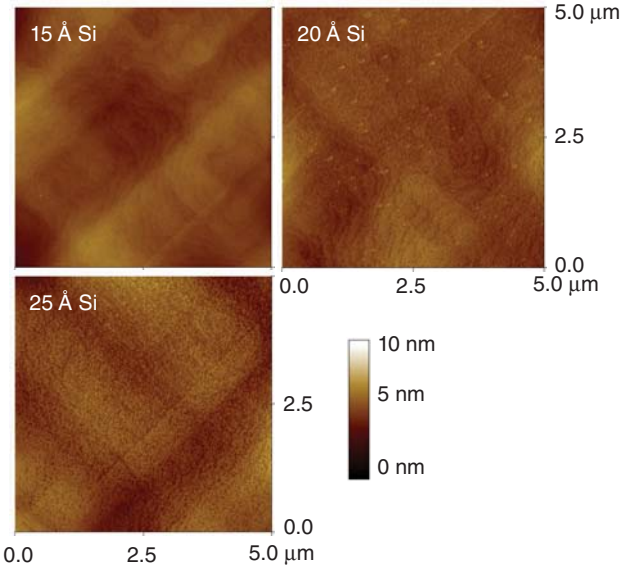

Figure 3.7 5 µm × 5 µm AFM images of the surface of thick annealed Ge layers capped by 15, 20, or 25 Å of Si. Image sides are more or less along the <100> directions. The associated rms roughness and *Z* ranges are equal to 5.4 and 42.1 Å (15 Å of Si), 4.5 and 47.3 Å (20 Å of Si) and 6.8 and 61.2 Å (25 Å of Si). From Ref. [26]. © IOP Publishing. Reproduced by permission of IOP Publishing. All rights reserved.

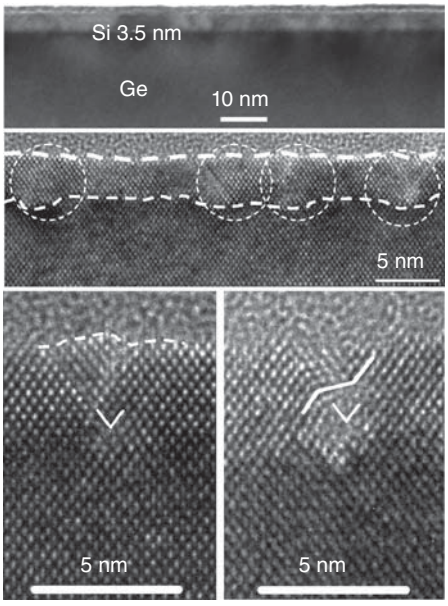

Figure 3.8 (Top row) Bright field, off Bragg, slightly under-focused image of a 35 Å thick Si layer sitting on top of a 2.8 μm thick, annealed Ge layer. (Bottom rows) High Resolution-Transmission Electron Microscopy (HR-TEM) images of the Si layer showing the presence of stacking faults and {111} twinnings in it. From Ref. [26]. © IOP Publishing. Reproduced by permission of IOP Publishing. All rights reserved.

small 3D islands a few tens of nanometers in diameter and 5–15 Å high. This Stranski–Krastanow growth mode is likely due to the high tensile strain in those thin Si layers. In order to dissipate some of it, elastic relaxation has apparently occurred, breaking for thickness above to 15 Å the conformal nature of the Si film. The Si atoms in the islands have tried to recover their bulk cubic structure (rather than having an in-plane lattice parameter much larger (due to the epitaxial relationship with Ge) than the perpendicular one).

Finally, we have imaged in cross-sectional TEM a 35 Å thick Si film grown (using the above-mentioned protocol) on top of an annealed Ge thick layer. Micrographs can be found in Figure 3.8.

The numerous Stacking Faults (SFs) observed in Figure 3.8 are most likely the result of the dissociation of perfect 60° misfit dislocations (with a $a_{Si}/2 < 101 >$ Burger's vector, a_{Si} being the Si lattice parameter). Those dislocations, initially nucleated as dislocation semi loops at the surface of the growing Si layer, have propagated toward the Si/Ge interface. They might also have come from the dislocated Ge layer underneath. Because of the tensile strain, they have then dissociated into 30° and 90° partial dislocations ($a_{Si}/6 < 211 >$ and $a_{Si}/2 < 1\bar{1}2 >$ Burger's vectors, respectively), which have then propagated (the 30° leading and the 90° trailing) on {111} planes, leaving in their wake SFs [41]. Our 35 Å thick Si layer is thus most definitely plastically relaxed.

3.4 SEG of Ge in Cavities at the End of Optical Waveguides

Several problems have to be circumvented in order to fabricate high performance, near infra-red Ge PDs on SOI substrates. First of all, the several hundreds of nanometers deep cavities at the end of optical waveguides have to be selectively filled with Ge. The use of Si_3N_4 as a masking material around those cavities is then forbidden. Poly-Ge would indeed be deposited on top of it (at least with GeH_4 as the germanium gaseous precursor, as here). This is to some extent not the case with SiO_2 (even with more than 1 μm thick Ge layers grown in the said cavities). Low growth pressures (20–100 Torr here) are otherwise expected to yield higher selectivity and should be preferentially used. With a direct coupling scheme, the floor of the cavities and the bottom part of the sidewalls are made of Si. Meanwhile, the top part of the sidewalls is made of SiO_2, the masking material. Ge layers will then have to be thick enough to ensure a full coupling between the Si waveguide and Ge at the cavity edges, where faceting might occur [2] (i.e., no deleterious air gap due to facets at that specific location). Thickness control is another troublesome problem. Severe global and local loading effects (i.e., increase of the growth rate when switching from blanket to patterned wafers, and, on patterned wafers, when moving from large, dense Si windows to small, isolated Si windows) are indeed expected with Ge SEG [42]. Finally, the crystalline quality of the Ge layer should be as high as possible (to reduce the PD dark current), which is far from being trivial given the 4.2% lattice mismatch between Ge and Si. Threading dislocation densities, of the order of $5 \times 10^7\,cm^{-2}$ for more than 1 μm thick Ge layers grown on blanket Si(001) using a 400 °C/750 °C scheme, can be brought down by a factor of ~5 thanks to HT thermal cycling [26]. Care should however be paid to the thermal budget, as Si atoms coming from the substrate will then penetrate into the Ge layer, leading to significant absorption losses [28].

We thus typically proceed as follows. A ("HF-last" wet cleaning/*in situ* H_2 bake at 850 °C for 2 min) surface preparation is first of all used to get rid of native oxide and contaminants on the cavities' floors and Si sidewalls. GeH_4 is then flown at 400 °C, 100 Torr in our 200 mm RP-CVD tool in order to accommodate, in a several tens of nanometers thick, rather flat Ge layer, the lattice mismatch between Ge and Si. Although the growth front is as expected a bit rough [28], faceting is not present at that stage even when the growth time is five times that usually used to that end (i.e., 300 s instead of 60 s). This is clearly illustrated by the top two 3D AFM images of Figure 3.9 and the bottom two sections of Figure 3.10.

Temperature is then slowly ramped-up ($2.5\,°C\,s^{-1}$) to 750 °C, at which the remainder of the Ge layer is grown in a few minutes (at 20 Torr). {111}, {113}, and higher Miller index faceting is then present at the cavity edges, as illustrated by the bottom 3D AFM images of Figure 3.9 and the top three sections of Figure 3.10. Ge overflow from the cavities (i.e., more than 1 μm layers, typically; rightmost two images of Figure 3.9) is aimed for in the end, in order to suppress any coupling issues and to reduce the defect density, which exponentially decreases with the

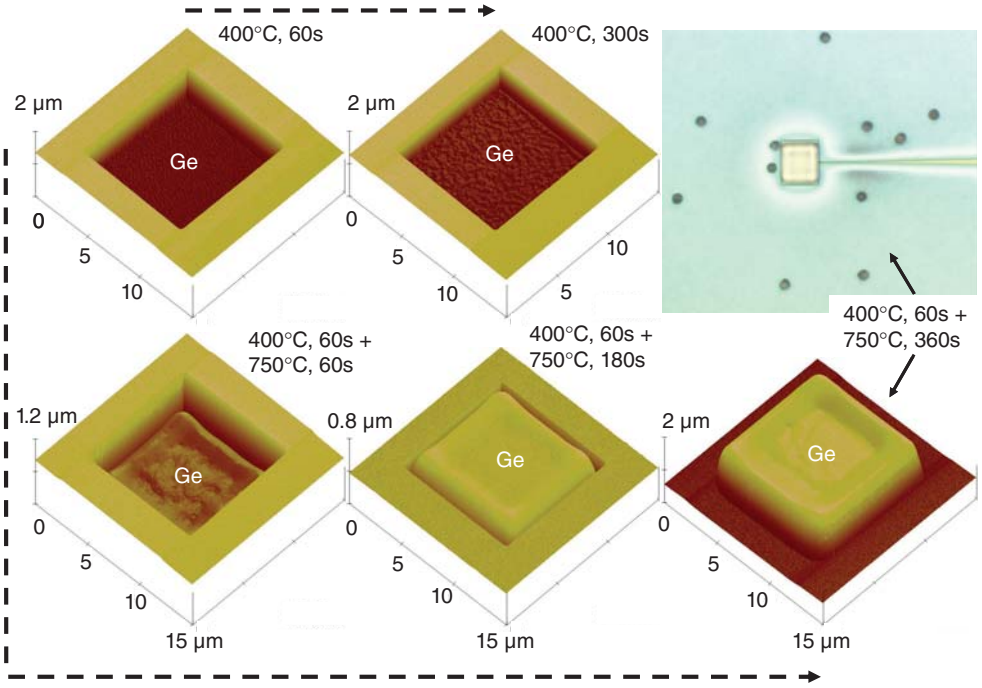

Figure 3.9 3D tapping mode atomic force microscopy images of 10 µm × 10 µm, initially ~150 nm deep cavities in bulk Si(001) surrounded by ~700 nm of SiO_2 (which acts as a hard mask; overall cavity depth close to 850 nm), this at various stages of their filling with Ge using a {400 °C, 100 Torr/750 °C, 20 Torr} process. Growth durations at those temperatures are provided next to each image. Poly-Ge nuclei on the SiO_2 hard mask are clearly seen in the top right optical microscopy image of a 10 µm × 10 µm cavity at the end of an optical waveguide after its overfilling with Ge. For the right two images, a 1 h H_2 annealing at 750 °C, 20 Torr was used after growth, as in real photo-detectors. From Ref. [4]. Reproduced by permission of OSA.

deposited thickness [25, 31, 32]. Thermal annealing at 750 °C for 1 h or very short thermal cycling between 750 and 890 °C is then performed under H_2 just after growth in order to further reduce the defect density without deleterious GeSi alloying. Finally, CMP is used in order to (i) get rid of the excess Ge at cavity locations and (ii) remove the poly-Ge nuclei present on the surrounding SiO_2. The imperfect selectivity is likely due to the use here of an initially 800 nm thick SiO_2 layer deposited at 520 °C then polished down to 700 nm, whose resulting surface is apparently of lesser quality than thermally grown SiO_2.

In order to conclude this section, we would like to say a few words about loading effects, which are huge. For the $F(GeH_4)/F(H_2)$ mass-flow ratio (2.5×10^{-4}) used here and the pattern layout probed in Figure 3.9, Ge growth rates were for 10 µm × 10 µm or 15 µm × 15 µm isolated windows 16–17 times those on blanket wafers, be it at 400 °C, 100 Torr or 750 °C, 20 Torr! We thus ended up with

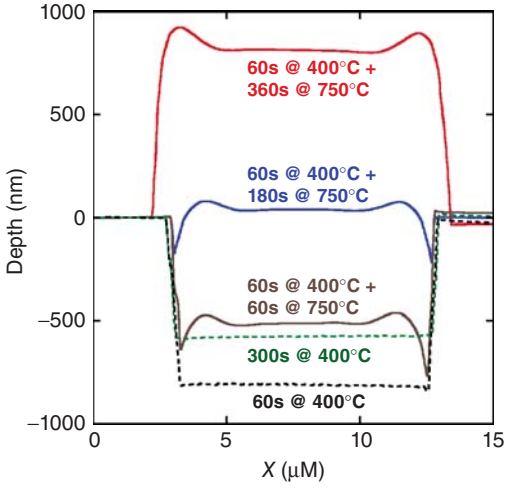

Figure 3.10 <110> sections obtained from Figure 3.1 AFM images showing the flatness of the Ge layers grown at 400 °C together with the appearance of <113> and high Miller indexes ({1110}, and so on) facets as soon as growth proceeds at 750 °C. When Ge overflows from the cavity, {111} steeper facets are then present at the very edges of the resulting "hut-like" structure. From Ref. [4]. Reproduced by permission of OSA.

~45 and 260 nm min^{-1} growth rates, respectively. Loading effects in similar dimension cavities but other chip designs were found to be in the 10–60 range. This thus means that a specific growth rate calibration is mandatory each time the lithography mask layout is changed.

3.5
Fabrication, Structural, and Electrical Properties of Compressively Strained Ge-on-Insulator Substrates

One major drawback of the LT/HT approach presented above is the defect density in the Ge layer. Threading dislocations density in thin or thick Ge layers grown directly on Si is indeed superior or equal to 10^7 cm^{-2}, even with HT cyclic anneals. We have thus decided to use thick $Si_{0.15}Ge_{0.85}$ virtual substrates (VSs) together with several chemical mechanical polishing (CMP) steps [18] as templates for the growth of low defect density, compressively strained Ge layers. Stopping the Ge concentration grading at 85% presents several advantages. First of all, the TDD in such VS is of the order of 10^5 cm^{-2} only. This is linked to the confinement of most of the misfit dislocations inside the graded SiGe layers. Going all the way to pure Ge would have induced a factor of roughly 10 increase in TDD, as dislocation nucleation is promoted in pure Ge [18, 43]. Second, several tens of nanometer thick compressively strained Ge layers can be grown pseudomorphically on those

slightly lower lattice parameter SiGe VS. They can then be transferred by the SmartCut™ process onto oxidized Si wafers, resulting in compressively strained GeOI (c-GeOI) substrates. Hole mobilities definitely higher than in fully relaxed Ge are expected in such strained layers, which is a strong asset [44–46]. Third, the bowing occurring when depositing SiGe on one side only of Si wafers in industrial single wafer reactors will be less if grading to 85% of Ge (instead of 100%).

3.5.1 The c-Ge on $Si_{0.15}Ge_{0.85}$ Process Flow

One major problem when growing thick, relaxed SiGe or Ge layers on a Si substrate is the wafer curvature. Epitaxial layers indeed grow (due to the design of single wafer industrial reactors) on one side only of a Si substrate. This leads to the appearance of a severe wafer bowing for high Ge content SiGe VS or thick Ge layers, as illustrated in Figure 3.11a. The SiGe VS considered here consisted in linearly graded (~8%Ge/μm) SiGe layers capped by roughly 1 μm thick constant Ge content SiGe layers. SiGe VS with a Ge content exceeding 30% have a concave shape, with a bow which monotonously decreases with the Ge content, reaching – 250 μm for 85% of Ge. Such a bow, which is roughly two times the one associated to 2.5 μm pure Ge layers grown directly on top of Si, is too large for subsequent wafer handling and bonding.

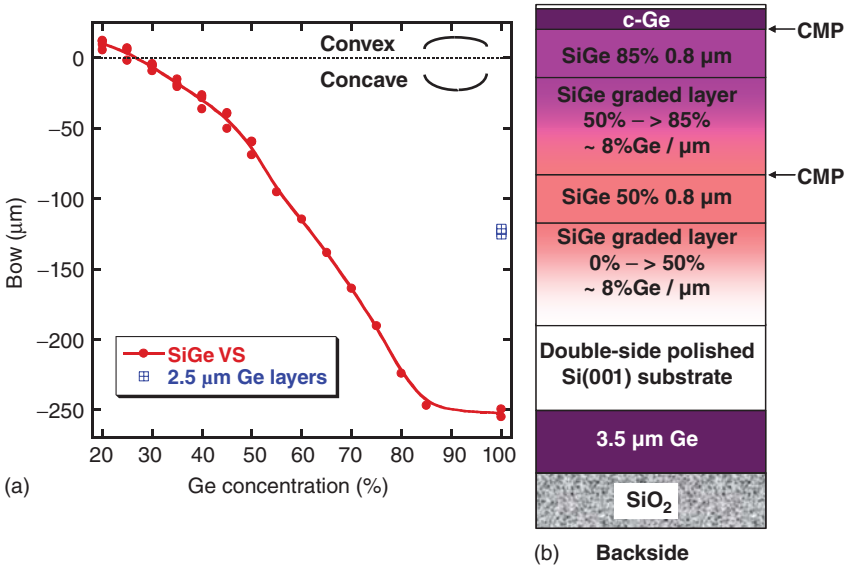

Figure 3.11 (a) Wafer bowing as a function of the Ge content of the top layer of SiGe virtual substrates or for pure Ge thick layers grown directly on Si. A positive (a negative) value of the bow means that the wafer is convex (concave). (b) Schematics of the c-Ge on SiGe 85% VS structure. From Ref. [83]. © IOP Publishing. Reproduced by permission of IOP Publishing. All rights reserved.

We have thus used the following approach in order to compensate that bow. We have started from Si(001) wafers polished on both sides and proceeded as follows:

1) After 1100 °C, 2 min. H_2 bakes, we have grown on the *front sides* high quality $Si_{0.5}Ge_{0.5}$ VS (TDD $\sim 10^5$ cm^{-2}) thanks to the use of HTs (900 °C from a few % up to ~35% of Ge, 850 °C for Ge contents higher than 35%) and low grading rates (~8%Ge/μm) [47]. At that stage, the mean value of the bow was −67 μm (concave shape).
2) We have capped the $Si_{0.5}Ge_{0.5}$ VS with 500 nm of SiO_2 (in order to protect both the SiGe layers and the handling tools).
3) After an "HF-last" wet cleaning and a 850 °C, 2 min *in situ* H_2 bake (in order to get rid of native oxide) [48], we have then deposited ~3.5 μm of Ge at 400 °C/750 °C on the *back sides*. After this, the wafers' shapes changed from concave to convex, with a mean +106 μm bow.
4) The Ge layers sitting on the back sides have then been capped by 1 μm of SiO_2 deposited at LT (350 °C). The 500 nm of SiO_2 protecting the front sides (i.e., the $Si_{0.5}Ge_{0.5}$ VS) have then been removed thanks to concentrated Hydrofluoric Acid in a single wafer dedicated cleaning tool (that sends chemical products on one side only of wafers). After those two steps, the mean bow was +14 μm.
5) The *front side* surface cross-hatch inherent to SiGe VS [47] has then been suppressed thanks to CMP steps followed by a dedicated wet cleaning [49] in order to recover a smooth surface. Because ~0.4 μm of $Si_{0.5}Ge_{0.5}$ was removed, the bow decreased to +10 μm.
6) After a "HF-last" wet cleaning and a 850 °C, 2 min *in situ* H_2 bake (in order to get rid of native oxide), we have grown at 850 °C on the $Si_{0.5}Ge_{0.5}$ VS a SiGe layer whose Ge content was linearly graded from 50 up to 85%, capped by a more than 1 μm thick $Si_{0.15}Ge_{0.85}$ layer (expected TDD: a few 10^5 cm^{-2}) [18].[2)] The mean bow was at that stage −131 μm.
7) We have then suppressed the surface cross-hatch that had reappeared [18] thanks once again to CMP (~0.4 μm of $Si_{0.15}Ge_{0.85}$ removed). After this, the final mean bow was equal to −119 μm, a value very close to the one of 2.5 μm thick Ge layers grown directly on Si(001) (−125 μm, see Figure 3.11). We were thus able (in the following) to use almost the same process steps than the ones used for pure Ge to bond the c-Ge/$Si_{0.15}Ge_{0.85}$ VS stacks onto oxidized Si wafers.
8) We have then proceeded with the growth of various thickness compressively strained Ge layers (sometimes capped with 2 nm of Si), whose structural properties will be discussed in the following section. The surface preparation prior to it was rather specific: (i) a robust "HF-last" wet cleaning (i.e., HF diluted at 1% in water (instead of 0.2% previously), together with a dip time that would have removed 15 nm of thermal SiO_2 (instead of 3 nm previously)),

2) Care to adopt bake and growth temperatures definitely lower than the Ge melting temperature (928°C) in order not to be troubled by the bow compensating Ge layers sitting on the wafers' backsides.

in order to start from SiGe surfaces free of native oxide [50], followed by (ii) a 30 s H_2 bake at 850 °C, 20 Torr in order to minimize the surface roughening prior to its capping with Ge [51]. The c-Ge growth conditions were as follows: $T = 550$ °C, $P = 20$ Torr, $F(GeH_4)/F(H_2) = 7.917 \times 10^{-4}$. The associated growth rate was equal to 37 nm min^{-1} (from cross-sectional TEM images). The 550 °C/650 °C Si capping with SiH_2Cl_2 at 20 Torr was detailed above.

A schematic of the resulting structure can be found in Figure 3.11b.

3.5.2 Structural Properties of the c-Ge on $Si_{0.15}Ge_{0.85}$ Stacks as a Function of the Ge Layer Thickness

3.5.2.1 Surface Morphology

We have used tapping mode AFM to visualize the surfaces of (i) our polished $Si_{0.15}Ge_{0.85}$ VS and (ii) various thickness compressively strained Ge layers (capped for one of them with 2 nm of Si). Typical 20 µm × 20 µm images can be found in Figure 3.12. CMP has, as expected, enabled us to get rid of the surface cross-hatch inherent to $Si_{0.15}Ge_{0.85}$ VS (i.e., 2–3 µm spatial wavelength undulations running along the perpendicular <110> directions, with rms roughness and

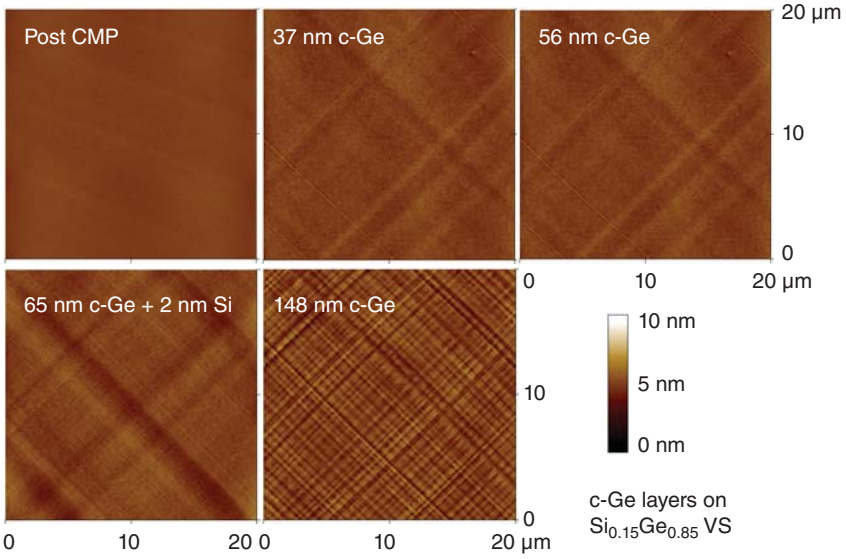

Figure 3.12 20 µm × 20 µm AFM images of the surface of polished $Si_{0.15}Ge_{0.85}$ VS prior to c-Ge deposition (top left) and after their capping by either 37, 56, 65, or 148 nm of compressively strained Ge layers (capped in the 65 nm case by 2 nm of Si). Image sides are more or less along the <100> directions. From Ref. [83]. © IOP Publishing. Reproduced by permission of IOP Publishing. All rights reserved.

Z ranges ($= Z_{max} - Z_{min}$) around 15 and 105 nm for 40 μm × 40 μm images, respectively). The resulting surface is indeed smooth (rms roughness = 0.16 nm and Z range = 2.2 nm) and featureless. Growing even thin (37 nm) c-Ge leads to a slight resurgence of the surface cross-hatch (with the same 2–3 μm spatial wavelength than the undulations of as-grown SiGe VS). "Ploughing" lines running along the <110> directions, which are most likely due to the propagation on {111} planes inside the c-Ge layers of the 60° threading dislocations present in the $Si_{0.15}Ge_{0.85}$ VS underneath (see thereafter), can also be seen on top of this low amplitude surface cross-hatch. Their linear density monotonously increases with the c-Ge layer thickness, from ~60 cm^{-1} (37 nm) up to ~150 cm^{-1} (56 nm) and finally ~1500 cm^{-1} (74 nm, AFM image not shown here). The surface morphology of the thickest c-Ge layer (i.e., 148 nm) is completely different from the one of thinner c-Ge layers. A much smaller spatial wavelength (~ 0.5 μm ⇔ 2–3 μm), which is likely due to a partial plastic strain relaxation (see thereafter) is indeed present on the surface of it. Finally, the surface morphology of the 65 nm c-Ge layer capped by 2 nm of Si has a morphology akin to the ones of the 56 and 74 nm thick c-Ge layers, except for the linear density of the "ploughing" lines, which is ~2250 cm^{-1}, that is, ~50% higher than the one associated to 74 nm c-Ge layers uncapped by Si. The higher value might be linked to the higher thermal budget called upon for the growth of the 65 nm c-Ge/2 nm Si cap that had helped threading dislocations move more into the c-Ge layer, thereby leaving more "ploughing" lines in their wake. Si capping has however no real impact of the surface roughness metrics, as the rms roughness and Z range of a 65 nm thick c-Ge layer with 2 nm of Si on top are equal to 0.37 and 3.7 nm, respectively.

3.5.2.2 Macroscopic Strain State

We have performed Omega-2Theta scans around the (004) and (224) diffraction orders (grazing incidence and grazing exit configurations) on some of the VS in order to gain access to the in-plane and perpendicular lattice parameters of (i) the constant composition $Si_{0.5}Ge_{0.5}$ layers on which the second part of the VS were grown and (ii) the constant composition $Si_{0.15}Ge_{0.85}$ layer sitting on top of the VS. From these data, we extracted the Ge content in those thick layers and their macroscopic degree of strain relaxation $R = (a^{\parallel}_{SiGe} - a_{Si})/(a^{bulk}_{SiGe} - a_{Si})$, $a^{\parallel}_{SiGe}$, a^{bulk}_{SiGe}, and a_{Si} being the in-plane lattice parameter of the SiGe layer, the bulk lattice parameter of a same Ge content SiGe layer and the lattice parameters of Si, respectively (formalism in Ref. [52]). The intermediate constant composition SiGe layers are fully relaxed ($R = 100.0\%$) and have a 51.1% a mean Ge content. Owing to differences in thermal dilation coefficients between Ge and Si [29], the top SiGe layers are slightly tensily strained ($R = 102.8\%$), with a 84.5% mean Ge content really close to the targeted one. Such a R value is very much in line with those reported in Ref. [18] for high Ge content SiGe VS.

We have plotted in Figure 3.13 the Omega-2Theta scans around the (004) diffraction orders for various thickness c-Ge layers grown on top of our VS. Several peaks which are assigned to (from low to high incidence angles) the c-Ge layer, the $Si_{0.15}Ge_{0.85}$ layer, the $Si_{0.49}Ge_{0.51}$ layer, and the Si(001) substrate

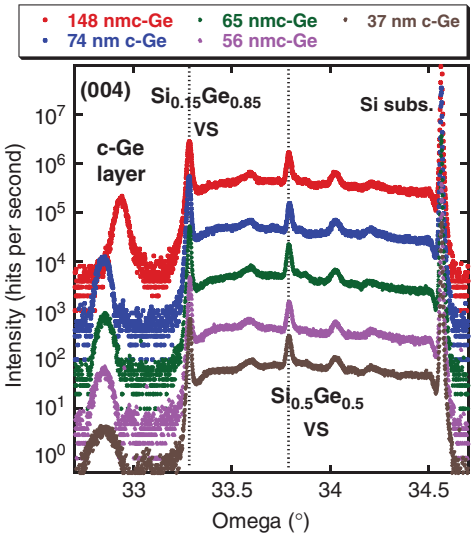

Figure 3.13 Omega-2Theta profiles around the (004) X-ray diffraction order associated to various thickness c-Ge layers (capped for the 65 nm thick c-Ge layer by 2 nm of Si) grown on top of polished $Si_{0.15}Ge_{0.85}$ VS. From Ref. [83]. © IOP Publishing. Reproduced by permission of IOP Publishing. All rights reserved.

can be seen in all profiles. The rather steady intensity between the latter three peaks is characteristic of a linear and well controlled Ge grading in our VS. We have extracted thanks to the Bragg's Law (i.e., $2(a_{Ge}^{\perp}/4)\sin\theta_{Ge} = \lambda$, $\lambda = 1.5406$ Å being the Cu $K\alpha_1$ wavelength) the perpendicular lattice parameter $a_{Ge}^{\perp}$ from the angular position θ_{Ge} of the peaks associated to the c-Ge layers. Values in the 5.6801 – 5.6808 Å range were found for c-Ge layers with thicknesses in the 37 – 74 nm range. The thickest c-Ge layer grown (148 nm) was plastically relaxed and characterized by a lower perpendicular lattice parameter (5.6671 Å).

These values are definitely larger than the bulk Ge lattice parameter ($a_{Ge}^{Bulk} = 5.65785$ Å) and the perpendicular lattice parameter of thick, cyclically annealed Ge layers grown directly on Si(001), which are always slightly tensily strained ($R = 104.5\%$ [26] => $a_{Ge}^{\perp} = 5.65025$ Å). Our Ge layers are thus definitely compressively strained.

3.5.2.3 Defect Density

We have decorated thanks to gaseous HCl the threading dislocations present in our $Si_{0.15}Ge_{0.85}$ VS [53]. After a "HF-last" wet cleaning, a polished VS has been submitted to an *in situ* H_2 bake at 650 °C for 2 min. followed by an exposure during 45 min to HCl at 475 °C, 20 Torr ($F(HCl)/F(H_2) = 3.75 \times 10^{-4}$). Around 200 nm of $Si_{0.15}Ge_{0.85}$ was removed during that etch (differential weighting). The resulting surface morphology has been studied by tapping mode AFM. A typical image can be found in Figure 3.14a. Square-based pits (mean side and depth: ~2.1 µm and 41 nm, respectively) can be observed together with a slight resurgence of the

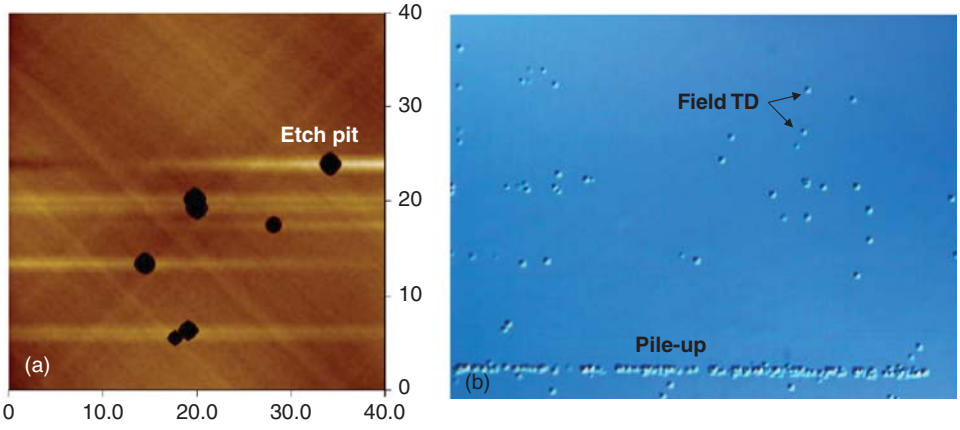

Figure 3.14 Typical tapping mode AFM (a) and optical microscopy (b) images of the surface of a polished $Si_{0.15}Ge_{0.85}$ VS after the *in situ* HCl etch at 475 °C of roughly 200 nm of the constant composition layer on top. Isolated and bunched together square-based etch pits at the emergence points of threading dislocations can clearly be seen. Image sizes: 40 μm × 40 μm (AFM) and 175 μm × 132 μm (OM). Image sides roughly along the <100> directions (AFM) or the <110> directions (OM). From Ref. [83]. © IOP Publishing. Reproduced by permission of IOP Publishing. All rights reserved.

surface cross-hatch along the <110> directions. We have used an optical microscope in order to image larger fields of view all over the wafer surface and obtain a meaningful TDD value. Threading dislocations were mostly of the field type (i.e., isolated one from the other). Piled-up threading dislocations were indeed present only in one of the roughly 30 130 × 175 μm^2 images captured (see Figure 3.14b). A 1.3×10^5 cm^{-2} TDD was associated to our polished $Si_{0.15}Ge_{0.85}$ VS (assuming that a HCl etch pit is associated to every threading dislocation). As targeted, we have reached a TDD value 2 orders of magnitude below the one of cyclically annealed Ge thick layers on Si(100).

We have also imaged in Plan-view TEM the $Si_{0.15}Ge_{0.85}$ VS capped by a 65 nm thick c-Ge layer with 2 nm of Si on top. Numerous lines along the <110> directions can definitely be seen in Figure 3.15 micrograph. They are most likely misfit segments located close to the c-Ge/$Si_{0.15}Ge_{0.85}$ VS interface. The threading arms of the 60° dislocations present in the SiGe VS underneath must have glided on {111} planes during its capping by compressively strained Ge, leaving in their wakes misfit dislocation segments along the <110> directions. They might also be due to the nucleation of new 60° dislocations in the more ductile c-Ge layer (then their propagation in it). We will indeed see in the following that the c-GeOI substrates are characterized by a $\sim 8 \times 10^5$ cm^{-2} TDD, versus 1.3×10^5 cm^{-2} in the $Si_{0.15}Ge_{0.85}$ VS used as template for the growth of c-Ge. The linear density of those misfit dislocation segments, 5.7×10^4 cm^{-1}, is much larger than the linear density of "ploughing" lines seen in AFM for the very same sample (2.25×10^3 cm^{-1}). The mean distance d_{mean} between misfit

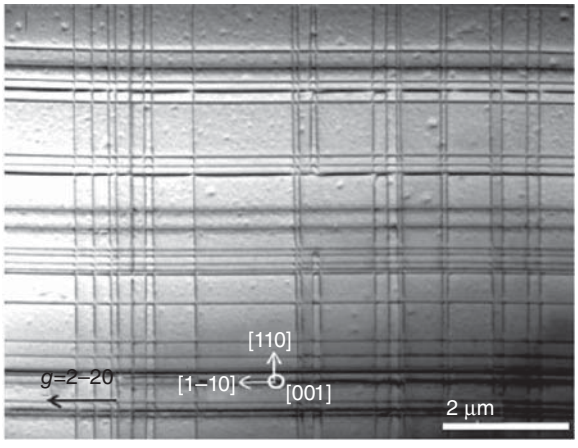

Figure 3.15 Bright-field plane view (001) image of the $Si_{0.15}Ge_{0.85}$ VS capped by a 65 nm thick c-Ge layer (2 nm of Si on top) taken with a $g = 2–20$ diffraction vector. From Ref. [83]. © IOP Publishing. Reproduced by permission of IOP Publishing. All rights reserved.

dislocations, which is given by $2 \times (\text{linear density})^{-1}$, is thus equal to 0.35 µm. Should those lines indeed be misfit dislocations coming from the propagation of perfect 60° dislocations, we would then have the following relationship: $\varepsilon^{\text{SiGe}}_{\text{in-plane}} = \frac{a^{\parallel}_{\text{Ge}} - a^{\parallel}_{\text{SiGe 85\%}}}{a^{\parallel}_{\text{SiGe 85\%}}} = \frac{|b_{\text{in-plane}}|}{d_{\text{mean}}} = \frac{|1/4a^{\text{Bulk}}_{\text{Ge}}<110>|}{d_{\text{mean}}} = 0.057\%$, $b_{\text{in-plane}}$ being the in-plane projection of the Burgers' vector associated to a 60° dislocation. We would then have $a^{\parallel}_{\text{Ge}} = 5.6275$ Å and thus $a^{\perp}_{\text{Ge}} = 5.6804$ Å, a value fully in agreement with XRD (5.6801 – 5.6808 Å, see Section 3.5.2.2).

3.5.3 Properties of the c-GeOI Substrates

3.5.3.1 Structural Properties

We have used the SmartCut™ process [9] to transfer the 65 nm Ge layer (capped by 2 nm of Si), compressively strained thanks to an epitaxy on a $Si_{0.15}Ge_{0.85}$ VS, on top of an oxidized Si substrate. After it, we ended up with the following stack (from top to bottom): 40 nm of c-Ge/2 nm thick Si layer/140 nm thick buried SiO_2 layer/Si substrate. The bottom 25 nm of the initially 65 nm thick c-Ge layer were indeed removed during polishing (after layer transfer), yielding an interfacial misfit dislocation free, flat, and high crystalline quality c-Ge layer. This is illustrated by the cross-sectional dark field TEM image of the overall stack and the two high resolution TEM close-ups (close to the c-Ge/buried oxide (BOX) interface and to the surface) shown in Figure 3.16.

Reciprocal space mapping around the (004) diffraction order was used to gain access to the perpendicular lattice parameter of the c-Ge layer, that is, 5.6724 Å. Such a value is slightly lower than that of c-Ge layers on SiGe 85% VS prior to

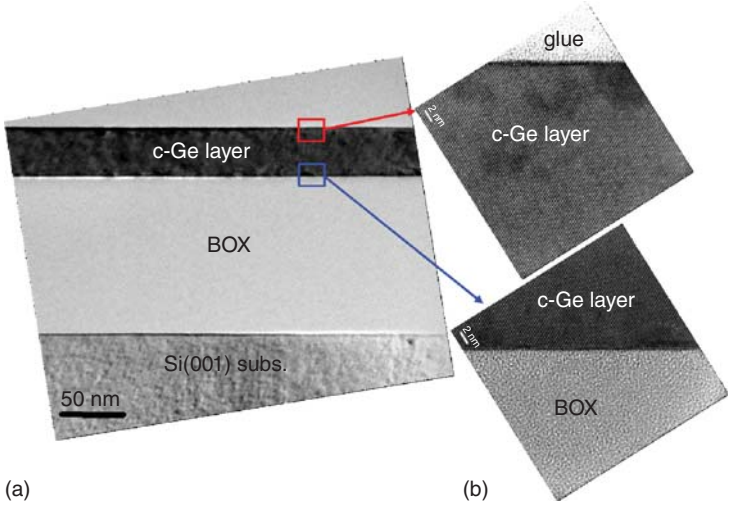

Figure 3.16 (a) Cross-sectional dark field TEM image of a 40 nm thick c-GeOI substrate (with a 140 nm thick buried oxide) and (b) HR-TEM close-ups on the c-Ge/glue and Ge/BOX interfaces. From Ref. [83]. © IOP Publishing. Reproduced by permission of IOP Publishing. All rights reserved.

transfer (5.6801 – 5.6808 Å), meaning that some of the compressive strain has been lost. Threading dislocations in GeOI and c-GeOI substrates were delineated in an oxidizing ambient. The TDD in conventional GeOI substrates, 10^7 cm^{-2}, was very similar to the one of the cyclically annealed 2.5 µm thick Ge layers on Si(001) used as donor wafers. By contrast, the TDD in our c-GeOI substrates, which is of the order of 8×10^5 cm^{-2}, was 20 times lower. It was however seven times higher than the one associated with $Si_{0.15}Ge_{0.85}$ VS (1.3×10^5 cm^{-2}). This is most likely due to the nucleation of new dislocations in the c-Ge layer during its growth and/or the layer transfer process (pure Ge is indeed more prone to that than a GeSi alloy [18, 43]). Finally, we have examined, using tapping-mode AFM, the surface of our c-GeOI substrates. As expected from Figure 3.16 TEM images, it was rather flat (rms roughness: 0.23 nm for 10 µm × 10 µm images), with however the presence of a very small amplitude and short spatial wavelength (~0.4 µm) surface cross-hatch along the <110> directions.

3.5.3.2 **Electrical Properties**

Hole mobility and threshold voltage in variable thickness c-GeOI substrates have been measured using the pseudo-MOSFET technique [54, 55]. This method, which is very simple, uses the natural upside-down MOS configuration of the semiconductor-on-insulator substrates. The semiconductor film represents the transistor body while the BOX is the gate oxide. The thick silicon substrate plays the role of gate and can be biased through a metal support to induce a

conducting channel at the interface between the film and the BOX. Depending on the sign of the gate bias V_G, inversion or accumulation channels can be activated. The source and drain are formed by applying two pressure-adjustable probes on the film surface. The pseudo-MOSFET characteristics in strong inversion or accumulation are correctly described by the elementary MOS transistor equations [55] for the linear region (drain voltage $V_D = 0.1\,V$). In order to avoid the first-order series resistance effects, we used the Y function $Y = I_D/\sqrt{g_m} = \sqrt{f_g C_{OX} V_D \mu_0}(V_G - V_{T(FB)})$ to extract the electrical parameters. I_D is the drain current, g_m is the transconductance, $f_g(= 0.75)$ is a geometrical factor, C_{OX} is the BOX capacitance, V_T is the threshold voltage for the inversion channel, V_{FB} is the flat-band voltage, acting as a "threshold" voltage, for the accumulation channel and μ_0 is the low-field mobility of electrons or holes. By plotting $I_D/\sqrt{g_m}$ versus V_G, we obtain the electron and hole mobilities from the slope, $\sqrt{f_g C_{OX} V_D \mu_0}$. The threshold and flat-band voltages are given by the intercept with the horizontal axis.

$I_D - V_G$ curves for various thickness c-GeOI wafers are shown as an example in Figure 3.17. The effective Ge/BOX interface passivation by Si (prior to bonding) enabled low threshold (V_T) voltages to be reached for c-Ge films thinner than 70 nm (0–6 V). This is a definite advantage compared with GeOI substrates obtained by the Ge enrichment technique, which are plagued by high V_T [56].

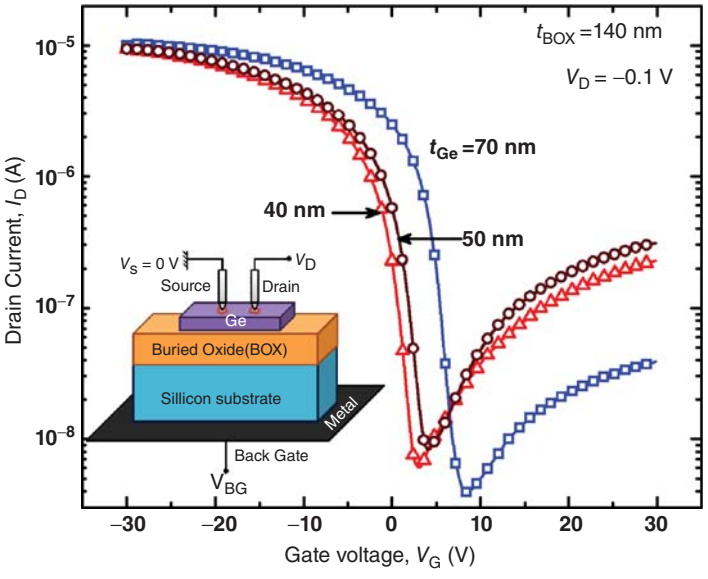

Figure 3.17 Pseudo-MOSFET $I_D - V_G$ curves for various thickness (t_{Ge} = 40, 50, and 70 nm) c-GeOI substrates (V_D = 100 mV source to drain voltage). Inset shows the configuration of pseudo-MOSFET measurements. From Ref. [83]. © IOP Publishing. Reproduced by permission of IOP Publishing. All rights reserved.

Hole mobility is high, reaching values (~300 cm^2/Vs) far superior to those in SOI. It remains excellent (~250 cm^2/Vs) even in 40 nm thick c-Ge films. The decrease of mobility with film thickness does not necessarily reflect a degradation in transport properties. It is due to the influence of the free, unpassivated surface where many charged defects subsist. As the film thickness decreases, the vertical electric field increases, leading to an apparent mobility degradation [57].

3.5.3.3 Benchmark

We have provided in Table 3.1 the perpendicular lattice parameter, the defect density, and the hole mobility in GeOI substrates of various origins in order to better apprehend the strengths and drawbacks of our c-GeOI substrates. GeOI substrates obtained through the transfer of the top part of thick Ge layers on Si [58], with bulk Ge substrates as donor wafers [59] or through the Ge enrichment technique [56] are tensily strained or neutral in terms of strain, which is quite different from our c-GeOI substrates, which are definitely compressively strained. Our c-GeOI substrates are characterized by a defect density tens to hundreds of times lower than enriched or SmartCut^{TM} (with Ge thick layers on Si as donors) GeOI substrates, which is highly beneficial for yield purposes. GeOI substrates with bulk Ge substrates are of course nearly perfect in terms of crystallinity, but very expensive and difficult to process (presence of Ge/Si dual wafers

Table 3.1 Benchmark of the structural properties and associated hole mobilities in various flavor GeOI substrates.

Nature	Ge layer thickness (nm)	Perpendicular lattice parameter (Å)	Defect density	Hole mobility from pseudo-MOSFET measurements[3]
Oxidized SOI [57]	50	5.431 No strain	Nil	160 $cm^2\ V^{-1}\ s^{-1}$
SmartCut^{TM} GeOI with thick Ge layers on Si as donor wafers [58]	55	5.650 Tensile strain	~10^7 cm^{-2}	250–350 $cm^2\ V^{-1}\ s^{-1}$
SmartCut^{TM} GeOI with bulk Ge as donor wafers [59]	200	5.658 No strain	Virtually nil	>350 $cm^2\ V^{-1}\ s^{-1}$
GeOI obtained through the Ge enrichment technique [56]	100	5.656 Slight tensile strain	~4×10^8 cm^{-2} (stacking faults)	400 cm^2
c-GeOI with a Si passivation of the c-Ge/BOX interface	50	5.672 Compressive strain	~8×10^5 cm^{-2}	260 $cm^2\ V^{-1}\ s^{-1}$

Please note that neither Ref. [58] nor Ref. [59] SmartCut^{TM} GeOI substrates had a Si passivation layer at the Ge/BOX interface (which would have reduced the pseudo-MOSFET hole mobility by a factor of up to 2).[3]

after bonding with vastly different thermal coefficients and brittleness of Ge compared to Si). Finally, it is rather clear from the data in Table 3.1 that moving from Si to Ge (whatever its fabrication technique) is beneficial in terms of hole mobility (gain by a factor of 1.5–2.5). Hole mobility comparison between the various GeOI substrates is rather difficult, however, as the Ge layer thickness and especially the back interface passivation scheme are different. Our c-GeOI substrates have indeed a 2 nm thick Si passivation layer inserted between the c-Ge layer and the BOX. The ~260 $cm^2 V^{-1} s^{-1}$ hole mobility associated to c-GeOI substrates is thus characteristic of two conduction channels in parallel: a high mobility one in the bottom part of the c-Ge layer and a lower mobility one in the Si passivation layer itself. A factor of 2 reduction of the hole mobility has recently been reported for SmartCut^{TM} GeOI substrates (obtained from thick Ge layers on Si) with a 1–2 nm thick Si passivation layer at the Ge/BOX interface [60]. Should the real hole mobility in the c-Ge layer be two times the one measured, it would then exceed the mobilities of SmartCut^{TM} GeOI substrates (250–350 and >350 $cm^2 V^{-1} s^{-1}$ with Ge on Si and bulk Ge as donors, respectively) or Ge enrichment GeOI substrates (~400 $cm^2 V^{-1} s^{-1}$).[3)]

3.6 Conclusion and Perspectives

We have described in the previous sections the growth protocols that are typically used to deposit (i) thick, fully relaxed Ge layers (on blanket Si(001) wafers and in the Si windows of patterned wafers) or (ii) thin, compressively strained Ge layers on GeSi VS. The resulting film and surface morphology, the strain state, and the defect density in such layers have been detailed and some mobility data presented.

We will conclude this chapter by saying a few words about "hot" topics that call upon thin or thick Ge layers that were not covered in the previous sections. Several hundreds of nanometers thick Ge layers selectively grown in deep, narrow cavities (with a Si floor and SiO_2 sidewalls) can benefit from Aspect Ratio Trapping [61–63], resulting in low defect density, relaxed layers that can be used as the core of high mobility Ge FinFETs [64] (presence of Ge(110) planes). A variant of this approach is to selectively grow Ge_xSi_{1-x} buffers (with x typically in the 70–85% range) instead of pure Ge in those cavities, followed by the epitaxy of thin, compressively strained Ge layers [65, 66], with therefore better transport properties than in unstrained Ge [67].

Such compressively strained Ge layers can otherwise be fabricated on blanket Reverse Graded Buffers (RGBs) [68]. In such stacks, thick, fully relaxed Ge layers are first grown on Si(001) wafers. RGBs, with Ge contents linearly *decreasing*

3) The buried oxide layer of enriched GeOI and conventional SOI substrates is of the thermal variety. Meanwhile, the upper part of the BOX layer of SmartCut^{TM} GeOI or c-GeOI substrates is deposited at low temperature. Hole mobilities extracted thanks to pseudo-MOSFET measurements (i.e., with the buried oxide acting as the gate dielectrics) are likely to be underestimated in SmartCut^{TM} GeOI or c-GeOI substrates, whose Ge/BOX interface is of lesser electrical quality than in enriched GeOI substrates.

from nearly 100 down to 80%, typically, are then deposited on those flat Ge films. Such RGBs, which are capped by a few hundreds nanometers of fully relaxed $Ge_{0.80}Si_{0.20}$, can then be used as templates for the growth of high hole mobility strained Ge layers [69].

The LT/HT approach used in Section 3.2 to grow Ge thick layers on blanket Si(001) substrates can also be employed on other crystallographic directions (e.g., on Si(011) and Si(111) substrates), with potentially higher electron and hole mobilities. Provided that the LT Ge layers are thin enough, rather smooth and high quality Ge(110) and Ge(111) thick layers can indeed be obtained [70]. However, specific defects and surface features coming from the intersection of the (011) or (111) surfaces with the threading dislocations' (111) gliding planes are found in such films [29, 70, 71].

Thick, fully relaxed Ge(001) layers, which can either be intrinsic or *in situ* phosphorous or boron-doped [72, 73], can otherwise be used as templates for the growth of high structural and electronic quality GeSn/SiGeSn heterostructures [74–77]. Alloying Ge or GeSi with Sn, a semimetal (i.e., $E_g = 0\,eV$) with a much larger diamond lattice parameter ($a_{Sn} = 6.489\,Å$) than Ge, can indeed be very interesting in terms of strain and bandgap engineering. One can notably use (i) thin, compressively strained GeSn layers (on Ge) as high hole mobility pMOSFET channels [78], (ii) embedded GeSn sources and drains as stressors in short gate length Ge pMOSFETs [79], relaxed GeSn/tensily strained Ge/relaxed SiGeSn heterostructures in vertical tunnel FETs [74], and so on. Thin or thick GeSn layers can otherwise be called upon in order to increase the responsivity and extend the operating wavelength of near infra-red PDs [80, 81]. Finally, high Sn content, relaxed GeSn layers (with a direct bandgap) can serve as the active medium of medium infra-red lasers [82].

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4
Heavy Doping in $Si_{1-x}Ge_x$ Epitaxial Growth by Chemical Vapor Deposition

Junichi Murota

4.1
Introduction

Atomically controlled processing for group IV semiconductors has become indispensable for the fabrication of ultrasmall metal-oxide-semiconductor devices and Si-based heterodevices, because high performance devices require atomic-order abrupt heterointerfaces and doping profiles as well as strain engineering to enhance the carrier mobility due to introduction of Ge into Si and heavy impurity doping into group IV semiconductors to lower the contact resistivity between metal and group IV semiconductor. Especially for processing involving surface reaction processes like chemical vapor deposition (CVD), the advancement of the process technology requires atomic-order surface reaction control. Because atomic level flatness of surfaces and interfaces needs to be maintained, low-temperature processing is indispensable in order to suppress thermal degradation such as unexpected reaction and impurity diffusion. Moreover, impurity gas molecules are adsorbed more easily at lower temperatures. An ultraclean environment is a critical requirement. Improvements in the quality of gases and equipment have enabled ultraclean low-temperature CVD processing for atomic-order control [1–4]. Our concept of atomic-level processing is based on atomic-order surface reaction control. The main idea of the atomic layer approach is the separation of the surface adsorption of reactant gases from the reaction process. Atomic-level control has been realized for epitaxy (Si, Ge), deposition (W, nitride), doping (P, B, C), and layer by layer etching [4–9].

In this chapter, *in situ* heavily doped $Si_{1-x}Ge_x$ epitaxial growth on the Si(100) surface in a SiH_4–GeH_4–dopant (PH_3, or B_2H_6, or SiH_3CH_3)–H_2 gas mixture and atomic-layer doping of B, P, and C by atomic layer formation of B, P, and C on $Si_{1-x}Ge_x$ (100) ($x = 0-1$) surface and subsequent $Si_{1-x}Ge_x$ cap layer deposition are reviewed, respectively. Moreover, the relationship between carrier concentration and impurity (B or P) concentration in the deposited layer and the influences of strain in $Si_{1-x}Ge_x$ epitaxial growth on the doping characteristics are described.

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4.2
In situ Doping of B, P, and C in $Si_{1-x}Ge_x$ Epitaxial Growth

4.2.1
In situ Doping Characteristics in $Si_{1-x}Ge_x$ Epitaxial Growth

The epitaxial growth of the $Si_{1-x}Ge_x$ films on the Si(100) substrates has been performed in a SiH_4–GeH_4–dopant (B_2H_6, PH_3, or SiH_3CH_3)–H_2 gas mixture by using an ultraclean hot-wall low-pressure CVD system. This system is made ultrahigh vacuum compatible. The details are described elsewhere [2, 4]. In order to prevent any contamination from the exhaust line, the wafers are transported through an N_2 purged transfer chamber into the reactor at a reactor temperature of about 100 °C, and then are heated-up to the surface treatment temperature or deposition temperature while purging with H_2 gas, and subsequently cooled-down to the low temperature $Si_{1-x}Ge_x$ ($x = 0-1$) deposition temperature and the heterostructure growth and *in situ* doping are performed [4, 6, 10]. The typical process sequence for $Si/Si_{1-x}Ge_x/Si$ heterostructure growth is shown in Figure 4.1. The typical pressure for the epitaxial growth is about 30 Pa. The oxygen and carbon pileups at the interface between the epitaxial layer and the Si substrate are drastically reduced below $5 \times 10^{11}\,cm^{-2}$ by thermal desorption and/or reduction due to Si source gas at 700–750 °C.

In the deposition of undoped $Si_{1-x}Ge_x$ on the Si(100) surface [4, 6, 10], the GeH_4 reaction rate increases monotonically with increasing GeH_4 partial pressure, while the SiH_4 reaction rate increases up to the maximum value and then decreases. With increasing SiH_4 partial pressure, the SiH_4 and GeH_4 reaction rates increase up to the maximum value and then decrease. The reaction rate is confirmed to be controlled by the surface reaction. Then, the SiH_4 and GeH_4 reaction rates are expressed by the Langmuir-type rate equation shown in Table 4.1 [6],

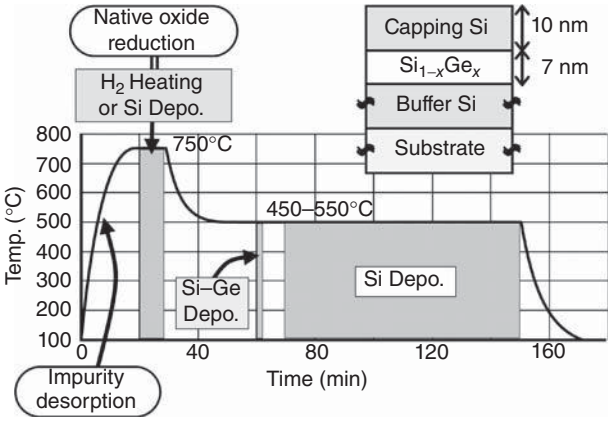

Figure 4.1 Typical process sequence for $Si/Si_{1-x}Ge_x/Si$ heterostructure growth using ultraclean hot-wall low-pressure CVD.

Table 4.1 Equations in the Langmuir-type adsorption and reaction scheme for formulating deposition rate, Ge fraction, and *in situ* doping in $Si_{1-x}Ge_x$.

SiH_4 and GeH_4 reaction rates

$$R_{Si} = \frac{k_1 P_{SiH_4} n_0}{1+(k_1/k_{Si})P_{SiH_4}}, \quad R_{Ge} = \frac{k_2 P_{GeH_4} n_0}{1+(k_1/k_{Si})P_{SiH_4}} \tag{4.1}$$

k_1, k_2: Adsorption rate constant of SiH_4 and GeH_4, respectively
k_{Si}: Reaction rate constant of SiH_4
n_0: Total adsorption site density
P_{SiH4}, P_{GeH4}: Partial pressure of SiH_4 and GeH_4, respectively

Deposition rate

$$R = R_{Si} + R_{Ge} \tag{4.2}$$

Ge fraction

$$x = \frac{R_{Ge}}{R_{Si}+R_{Ge}} = \frac{k_2}{k_1} \cdot \frac{P_{GeH_4}}{P_{SiH_4}+(k_2+k_1)P_{GeH_4}} \tag{4.3}$$

Rate constants of adsorption and reaction of SiH_4 and GeH_4

$$k_a n_0 = \sum_{i=1}^{3} k_{ai} n_0 c_i \ \frac{1}{1+K_{Di}P_D} \tag{4.4}$$

($a = 1, 2, \text{Si}$; $D = \text{P, B, C}$; $c_1 = (1-x)^2$, $c_2 = 2x(1-x)$, $c_3 = x^2$).
k_{ai}: Reaction rate constant at each pair site
P_D: Partial pressure of dopant gas
K_{Di}: Effective adsorption equilibrium constant of dopant molecules at each pair site

$$K_{Di} = \frac{k_{Di}}{K_{SDi}Rc_i+k_{-Di}} \tag{4.5}$$

k_{Di}: Adsorption rate constant of dopant molecules at each pair site
k_{-Di}: Desorption rate constant of dopant molecules at each pair site
K_{Sdi}: Effective segregation coefficient between the surface coverage of dopant molecules and the concentration of dopant incorporated in the depositing film at each pair site

Dopant concentration in $Si_{1-x}Ge_x$

$$C_D = \sum_{i=1}^{3} K_{SDi} c_i \frac{K_{Di}P_D}{1+K_{Di}P_D} \tag{4.6}$$

assuming that one SiH_4 or GeH_4 molecule is adsorbed at Si–Si, Si–Ge, or Ge–Ge pair sites on the (100) surface and decomposed there. The values of the effective rate constants for SiH_4 and GeH_4 at each site, $k_{ai}n_0$ (see Eq. (4) in Table 4.1) are obtained numerically by fitting the experimental data. These values are shown in Table 4.2 [6]. It is found that the SiH_4 and GeH_4 adsorption rate constants (k_1 and k_2) become larger at the bond site of the Si–Ge pair than those at the others, while the SiH_4 surface reaction rate constant (k_{Si}) becomes the largest at the bond site of the Ge–Ge pair.

In situ doping characteristics of B, P, and C in $Si_{1-x}Ge_x$ epitaxial growth can also be explained as shown in Table 4.1, assuming that one dopant molecule (B-hydride, P-hydride, or SiC-hydride) occupies one free surface site according to Langmuir's adsorption isotherm, that the site where the dopant molecule has been adsorbed becomes inactive for both the SiH_4 and GeH_4 adsorption/reactions on the surface, that such the dopant occupancy is different at the Si–Si, Si–Ge, and

Table 4.2 The fitting parameters $k_{1i}n_0$, $k_{2i}n_0$, and $k_{Sii}n_0$ at 550 °C on the (100) surface, calculated from Eqs (4)–(4) in Table 4.1 using the experimental data.

I	$k_{1i}n_0$ (cm min^{-1} Pa^{-1})	$k_{2i}n_0$ (cm min^{-1} Pa^{-1})	$k_{Sii}n_0$ (cm min^{-1})
1	24×10^{-8}	400×10^{-8}	12×10^{-8}
2	140×10^{-8}	600×10^{-8}	12×10^{-8}
3	40×10^{-8}	150×10^{-8}	1200×10^{-8}

$i = 1, 2,$ and 3 correspond to the Si–Si, Si–Ge, and Ge–Ge pair sites, respectively.

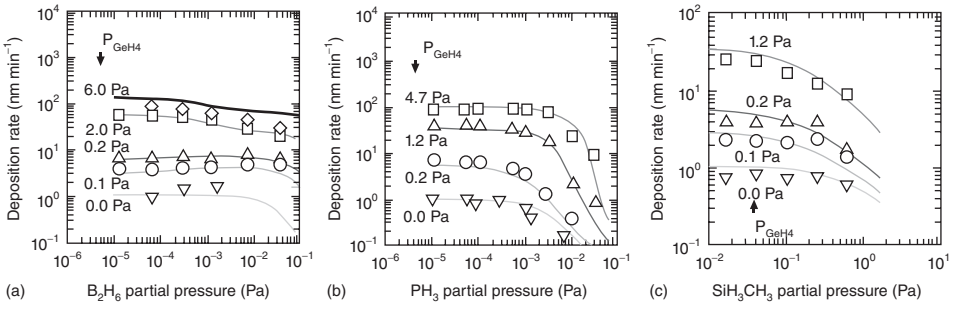

Figure 4.2 (a) B_2H_6, (b) PH_3, and (c) SiH_3CH_3 partial pressure dependences of the deposition rate. The solid lines are calculated from Eqs (4)–(4) in Table 4.1 with the fitting parameters in Tables 4.2 and 4.3. The total pressure and the SiH_4 partial pressure are 30 and 6.0 Pa, respectively. The deposition temperature is 550 °C.

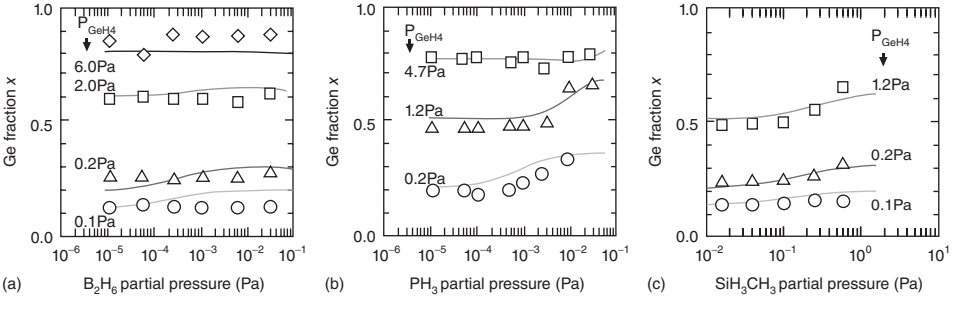

Figure 4.3 (a) B_2H_6, (b)PH_3, and (c) SiH_3CH_3 partial pressure dependences of the Ge fraction x. The solid lines are calculated from Eqs (4)–(4) in Table 4.1 with the fitting parameters in Tables 4.2 and 4.3. The total pressure and the SiH_4 partial pressure are 30 and 6.0 Pa, respectively. The deposition temperature is 550 °C.

Ge–Ge pair sites on the surface, and that the dopant incorporation in the grown film is determined by Henry's law [5, 6, 10].

The values of k_{Di}, k_{-Di}, and K_{SDi} in Table 4.1 are determined by fitting the experimental data in Figures 4.2–4.4 to Eqs (4)–(4) in Table 4.1 with the values shown in Table 4.2 [6]. The best values are shown in Table 4.3 [6]. Fairly good agreement

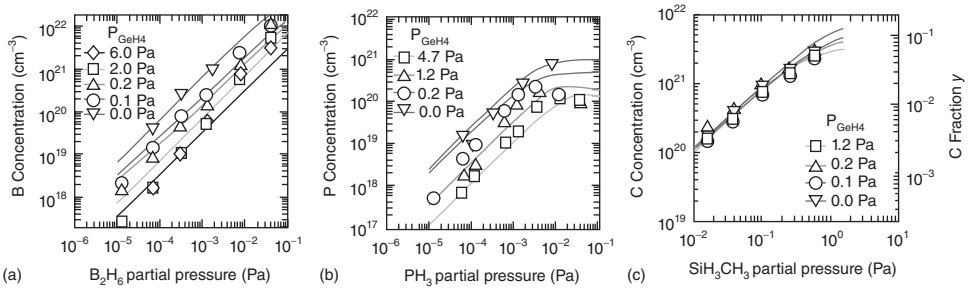

Figure 4.4 (a) B_2H_6, (b) PH_3, and (c) SiH_3CH_3 partial pressure dependences of the B, P, and C concentrations, respectively. The solid lines are calculated from Eqs (4)–(4) in Table 4.1 with the fitting parameters in Tables 4.2 and 4.3. The total pressure and the SiH_4 partial pressure are 30 and 6.0 Pa, respectively. The deposition temperature is 550 °C.

is obtained between all the experimental data and the calculated values as shown by solid lines in Figures 4.2–4.4.

In the case of B doping [6, 10], the deposition rate decreases with B_2H_6 addition at higher GeH_4 partial pressures (Figure 4.2a). The Ge fraction scarcely changes with the B_2H_6 addition (Figure 4.3a). The B concentration increases nearly proportionally with the B_2H_6 partial pressure up to the 10^{22} cm^{-3} range (Figure 4.4a), nevertheless all these films are single crystalline. The best fitting values listed in Table 4.3 shows that the effective segregation coefficient between coverage of B-hydride and the concentration of B incorporated in the deposited film K_{SB} becomes the smallest at the Si–Ge pair site. It is known from evaluation using Eq. (4) in Table 4.1 that the B_2H_6 adsorption rate constant K_{B2} at the Si–Ge pair site is the largest, and as a result with increasing B_2H_6 partial pressure, the weighted sums of the SiH_4 and GeH_4 adsorption rate constants, k_1 and k_2, evaluated by Eq. (4) decrease more compared to that of the SiH_4 reaction rate constant k_{Si}. This explains the decrease of the deposition rate with the B_2H_6 addition at high deposition rate at high Ge fraction.

Table 4.3 The fitting parameters k_{Di}, k_{-Di}, K_{SDi} on the (100) surface at 550 °C, calculated from Eqs (4)–(4) in Table 4.1 and the fitting parameters in Table 4.2 using the experimental data in Figures 4.2–4.4.

D	B			P			C		
I	1	2	3	1	2	3	1	2	3
	Si–Si	Si–Ge	Ge–Ge	Si–Si	Si–Ge	Ge–Ge	Si–Si	Si–Ge	Ge–Ge
k_{Di} ($\times 10^{15}$ cm^{-2} min^{-1} Pa^{-1})	100	300	200	50	80	10	3	50	30
k_{-Di} ($\times 10^{12}$ cm^{-2} min^{-1})	1000	20	20 000	100	1	1	2000	2000	2000
K_{SDi} ($\times 10^{19}$ cm^{-3})	3000	3	3000	100	10	10	1000	100	500

$i = 1, 2,$ and 3 correspond to the Si–Si, Si–Ge, and Ge–Ge pair sites.

In the case of P-doping [6, 10], the reduction of the deposition rate shifts to higher PH_3 partial pressures with increasing GeH_4 partial pressure (Figure 4.2b). The Ge fraction increases at higher PH_3 partial pressure (Figure 4.3b). The P concentration increases up to a maximum value and then decreases with increasing PH_3 partial pressure (Figure 4.4b). Calculating the effective adsorption equilibrium of PH_3 at each pair site K_{Pi} from Eq. (4) in Table 4.1 with the values in Table 4.3, the effective adsorption of PH_3 is the lowest at the Si–Si pair site. As a result, with the PH_3 addition, adsorption of SiH_4 and GeH_4 becomes a maximum at the Si–Si pair site and the k_2/k_1 value becomes larger, which results in the increase of the Ge fraction given by Eq. (4) in Table 4.1. Namely, the reduction of the deposition rate (Figure 4.2b) and the increase of the Ge fraction (Figure 4.3b) at higher PH_3 partial pressure are caused by more suppression of SiH_4 and GeH_4 adsorptions/reactions on the Si–Ge and Ge–Ge pair sites than on the Si–Si pair site. The maximum P concentration (Figure 4.4b) is explained by the saturation of PH_3 adsorption and the lower effective segregation coefficient (between coverage of P-hydride and the concentration of P incorporated in the deposited film) on the Si–Ge and Ge–Ge pair sites than on the Si–Si pair site given by the K_{SPi} values.

In the case of C-doping [6, 11], with increasing SiH_3CH_3 partial pressure, the deposition rate decreases depending on the Ge fraction (Figure 4.2c), the Ge fraction increases at a high SiH_3CH_3 partial pressure (Figure 4.3c) and the C concentration increases linearly up to about $10^{21}\,cm^{-3}$ (Figure 4.4b). These tendencies could be explained in the same manner as in the case of P doping as well as B doping using the equations in Table 4.1 and the fitting parameters in Tables 4.2 and 4.3.

These results demonstrate that the mechanism of growth and doping during $Si_{1-x}Ge_x$ epitaxial growth in the surface reaction limited regime can be described by the modified Langmuir-type adsorption and reaction scheme shown in Table 4.1.

4.2.2
Relationship between Carrier and Impurity (B or P) Concentrations in $Si_{1-x-y}Ge_xC_y$ Epitaxial Film

In the case of B-doped $Si_{1-x-y}Ge_xC_y$ epitaxial films with $y = 0.0054$ or lower deposited at 550 °C and B-doped Ge epitaxial films deposited at 350 °C [12], the carrier concentration is nearly equal to the B concentration (C_B) up to about $2 \times 10^{20}\,cm^{-3}$, and it tends to saturate to about $5 \times 10^{20}\,cm^{-3}$ at a C_B below $10^{22}\,cm^{-3}$, independently of the Ge fraction (Figure 4.5a) [12–14]. Discrepancy of the lattice constants from Vegard's law was observed at a higher C_B in the order of $10^{20}\,cm^{-3}$ and above, which corresponds with the saturation of the carrier concentration [13]. With increasing C fraction, the electrically inactive B atoms appear and tend to increase in number even at the lower C_B region [14].

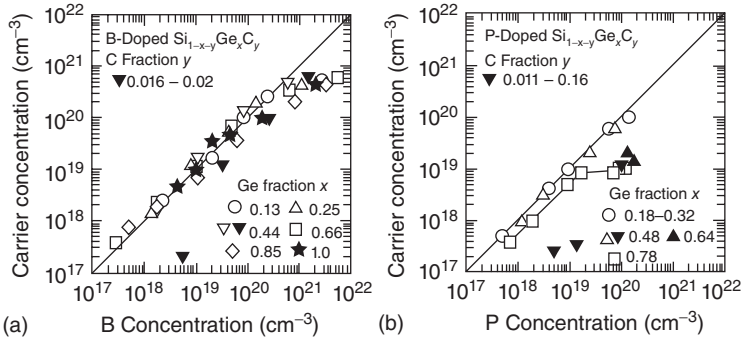

Figure 4.5 Dependences of carrier concentrations in $Si_{1-x-y}Ge_xC_y$ epitaxial films on (a) P and (b) B concentrations. $Si_{1-x-y}Ge_xC_y$ epitaxial films were deposited at 550 °C except for B-doped Ge epitaxial films deposited at 350 °C.

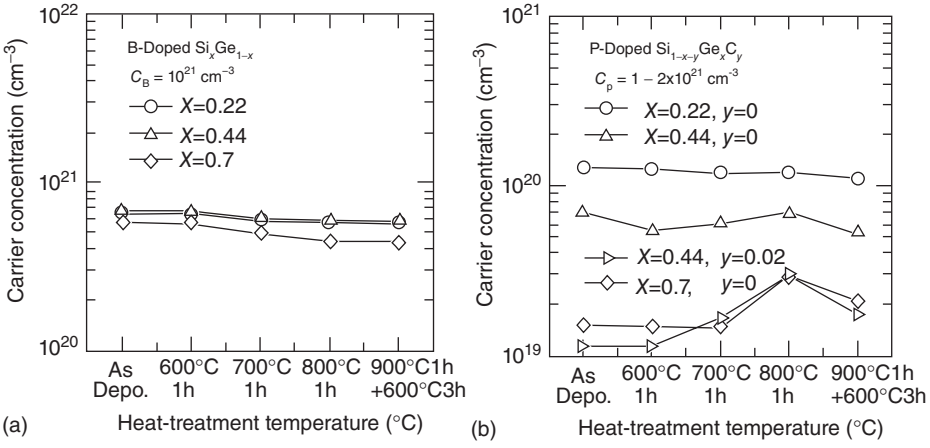

Figure 4.6 The heat-treatment temperature dependence of the carrier concentration in (a) B-doped $Si_{1-x}Ge_x$ films and (b) P-doped $Si_{1-x-y}Ge_xC_y$ films.

The carrier concentration in B-doped $Si_{1-x}Ge_x$ epitaxial film deposited at 550 °C with a high C_B of 10^{21} cm^{-3} decreases with increasing the heat-treatment temperature up to 800 °C for 1 h (Figure 4.6a) [15]. The decrease of the carrier concentration becomes slightly larger with increasing the Ge fraction. By the subsequent heattreatment at a low temperature of 600 °C for 3 h, the carrier concentration does not recover. Because the lattice constant of the film became larger after the heattreatment at 800 °C for 1 h [15], it is suggested that the epitaxial film is grown in a non-equilibrium for B and B clustering proceeds by heattreatment.

In the case of P-doped $Si_{1-x-y}Ge_xC_y$ epitaxial films deposited at 550 °C, the carrier concentration of the film with low Ge and C fraction ($x \leq 0.48, y \leq 0.0046$) is nearly the same as the P concentration (C_P) up to about 2×10^{20} cm^{-3} (Figure 4.5b) [16, 15, 6]. In the case of the film with higher Ge fraction, the electrically inactive P

atoms are observed independently of C_P, and when $x = 0.64$ and 0.78, the carrier concentration tends to saturate to about $10^{19}\,cm^{-3}$ at a higher C_P of about $2 \times 10^{20}\,cm^{-3}$. This means that the P-doped $Si_{1-x}Ge_x$ films with higher Ge fraction have the lower solid solubility of electrically active P. With increasing the C fraction in the film ($y \geq 0.0048$), the electrically inactive P atoms tend to increase [16, 15]. This means that the P-doped $Si_{1-x-y}Ge_xC_y$ films with higher Ge and C fraction have a lower solid solubility of electrically active P.

The carrier concentration in P-doped $Si_{1-x-y}Ge_xC_y$ film with a high C_P of $10^{20}\,cm^{-3}$ deposited at 550 °C scarcely changes with the heattreatment at a Ge fraction of $x = 0.44$ or below (Figure 4.6b). At a high Ge fraction of $x = 0.7$, the carrier concentration become two times higher than that of as-deposited film after heattreatment at 800 °C for 1 h [15]. Because the lattice constant of the film became smaller by heattreatment, it is suggested that the solid solubility of electrically active P atoms becomes higher due to the generation of substitutional P atoms at higher heat-treatment temperature. By subsequent heattreatment at lower temperature of 600 °C for 3 h, the carrier concentration decreases and the lattice constant slightly becomes larger again [15]. These results suggest that many of the P atoms are located at the substitutional site more preferentially at higher heat-treatment temperature, whereas they are located at the interstitial site at lower heat-treatment temperature. In the case of $Si_{0.54}Ge_{0.44}C_{0.02}$ film, the carrier concentration becomes 2.7 times higher than that of as-deposited film as shown in Figure 4.6b. The lattice constant becomes larger after heattreatment at 800 °C for 1 h, although the lattice constant of the undoped $Si_{0.54}Ge_{0.44}C_{0.02}$ film scarcely changes [15]. From these results, it is suggested that the generation of substitutional P atoms is enhanced by the localization of C atoms into the interstitial site due to heat treatment. It may be mentioned that the carrier concentration above $10^{20}\,cm^{-3}$ and higher solid solubility of P for P-doped Ge result from higher temperature processing [17].

4.3 Atomic-Layer Doping in $Si_{1-x}Ge_x$ Epitaxial Growth

Self-limiting formation of one to three atomic layers of group IV or related atoms in the thermal adsorption and reaction of hydride gases (SiH_4, GeH_4, NH_3, B_2H_6, PH_3, CH_4, and SiH_3CH_3) on $Si_{1-x}Ge_x$ (100) surface were generalized based on the Langmuir-type model [6, 18]. In many cases, hydride molecules are adsorbed and react simultaneously on the surface as shown in Figure 4.7 [6]. Moreover, atomic-layer doping is performed by $Si_{1-x}Ge_x$ epitaxial growth on N, B, P, or C atomic layer alreadyformed on the $Si_{1-x}Ge_x$ (100) surface [6, 7, 18–21]. The typical process sequence is shown in Figure 4.8.

In this section, we review heavy atomic-layer doping of B, P, and C by atomic layer formation of B, P, and C on $Si_{1-x}Ge_x$ (100) surface and subsequent Si cap layer deposition, respectively. Moreover, the influences of strain in $Si_{1-x}Ge_x$ epitaxial growth on the doping characteristics are described.

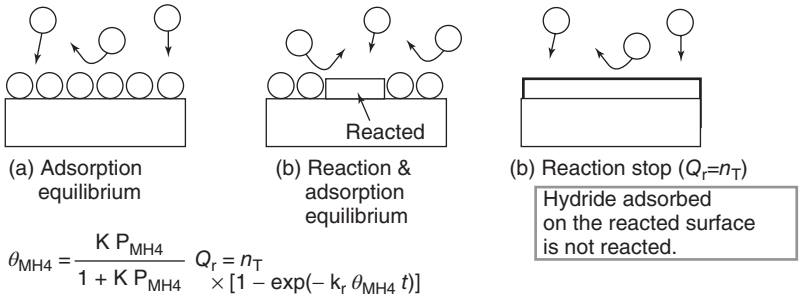
Reacted
(a) Adsorption equilibrium
(b) Reaction & adsorption equilibrium
(b) Reaction stop (Q_r=n_T)
Hydride adsorbed on the reacted surface is not reacted.
$\theta_{MH4} = \frac{K P_{MH4}}{1 + K P_{MH4}}$ $Q_r = n_T \times [1 - \exp(-k_r \theta_{MH4} t)]$

Figure 4.7 Schematic image of self-limited reaction of hydride for atomic-order growth based on Langmuir-type model. θ_{MH4} is the coverage of MH_4 molecules on the surface, K the equilibrium constant between the adsorbed MH_4 amount and MH_4 partial pressure, Q_r the site density where adsorbed MH_4 reacted, n_T the total adsorption site density at the surface, and k_r the reaction rate constant of MH_4 on the surface.

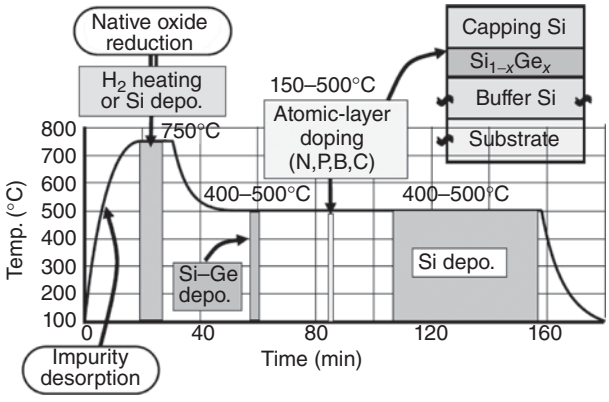

Figure 4.8 Typical process sequence for atomic-layer doping using an ultraclean hot-wall low-pressure CVD.

4.3.1
Boron Atomic-Layer Doping in $Si_{1-x}Ge_x$ Epitaxial Growth

4.3.1.1 Surface Reaction of B_2H_6 on $Si_{1-x}Ge_x$(100)

By B_2H_6 exposure on the Si(100) at 180 °C (Figure 4.9) [21], the B atomic amount tends to saturate self-limitedly at around $1.4 \times 10^{15}\,cm^{-2}$ (2 atomic layer (AL)). At 500 °C, the B atomic amount increases with B_2H_6 exposure time and exceeds 2 AL. It is clear that continuous B_2H_6 reaction at 500 °C proceeds with H desorption on B atoms. Typical B 1 s spectra of x-ray photoelectron spectroscopy (XPS) obtained from the B AL with B atomic amount with $6 \times 10^{14}\,cm^{-2}$ on Si(100) after air exposure (Figure 4.10) shows that an elemental B peak appears at around 187–190 eV [22] for both the temperatures of 180 and 500 °C, while the peak for 500 °C is smaller than that for 180 °C. A B oxide peaks at 190–195 eV [22] are observed for 500 °C but not for 180 °C. This supposes that H adsorption on B

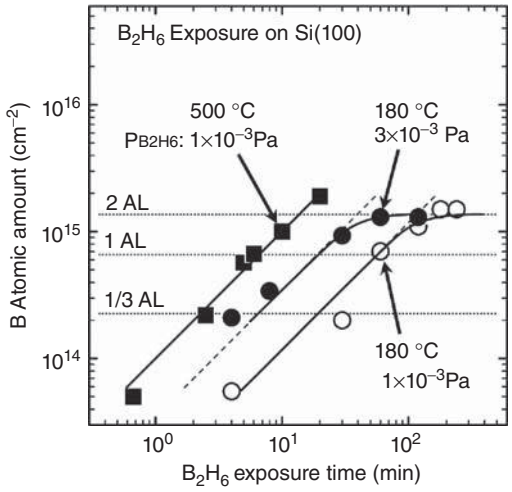

Figure 4.9 B_2H_6 exposure time dependence of B atomic amount on Si(100) at 180 and 500 °C, obtained by XPS.

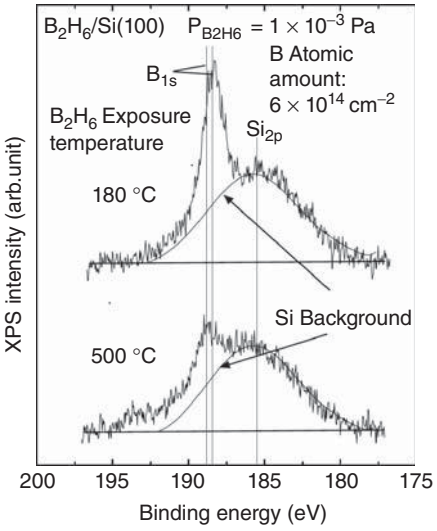

Figure 4.10 B_{1s} XPS after air exposure from B atomic-layer on Si(100) formed at 180 and 500 °C with B atomic amount of about 6 × 10^{14} cm^{-2}.

atoms protects B oxidation. Therefore, it is suggested that the H adsorption on the B AL maintains at 180 °C whereas H desorption from the B AL proceeds at 500 °C. In the case of BCl_3 exposure on $Si_{0.7}Ge_{0.3}$(100) and Ge(100) [23], B atomic amount tended to increase beyond 1 AL by using H_2 carrier gas at 450 °C. 1/3 to 1/2 atomic layer formation was achieved self-limitedly with high Cl coverage on the

surface by using Ar carrier gas at 450 °C. It was also found that the Cl atoms on B adsorbed $Si_{1-x}Ge_x(100)$ are effectively removed by H_2 exposure at 450 °C.

4.3.1.2 $Si_{1-x}Ge_x$ Epitaxial Growth over B Atomic Layer Already Formed on the (100) Surface

By Si epitaxial growth with SiH_4 reaction at 500 °C on top of the B atomic layer of about 7×10^{14} cm^{-2} formed with B_2H_6 reaction at 180 °C on Si(100) surface, most of the incorporated B atoms are confined within a 1 nm-thick region (Figure 4.11). The total B atom amount is near the initial B atomic amount before the subsequent Si epitaxial growth [20], but the sheet carrier concentration is as low as 1.7×10^{13} cm^{-2}. The electrical inactive B could be a result of clustering of surface B atoms just before Si deposition at 500 °C. It is wellknown that B clustering reduces the electrical activity of B in Si. By heavy B doping, strain could be induced [46]. For *in situ* B-doped Si epitaxial growth on about 0.5%-tensile-strained Si(100)-on-insulator (SOI) at 550 °C using SiH_4 and B_2H_6, the B concentration region in which carrier concentration is almost equal to the B concentration was lower, compared with that on the unstrained SOI [24]. For example, the carrier concentrations are 10^{20} cm^{-3} for B concentration (C_B) of 10^{20} cm^{-3} and 2×10^{20} cm^{-3} for C_B of 10^{21} cm^{-3} in B-doped Si on the unstrained SOI and 3×10^{19} cm^{-3} for C_B of 7×10^{19} and 1.5×10^{20} cm^{-3} for C_B of 1.5×10^{21} cm^{-3} in that on the tensile-strained SOI. This means that, for *in situ* B-doped Si epitaxial growth, the substitutional B and the interstitial B concentrations in the unstrained Si is higher and lower

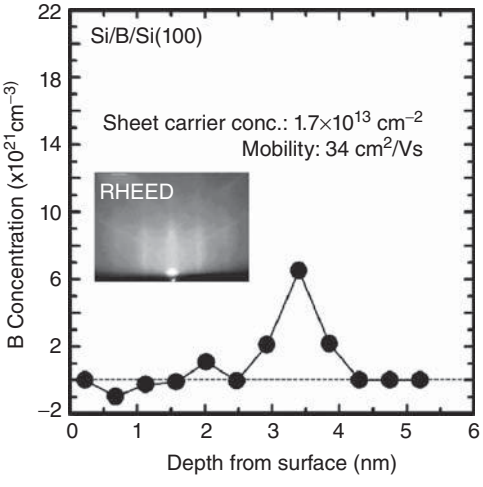

Figure 4.11 Depth profile of B concentration, carrier concentration, and mobility in the B atomic-layer doped Si films on Si(100). The Si cap layer deposition at 500 °C was performed after low-temperature SiH_4 exposure at 180–300 °C on top of B atomic layer of about 7×10^{14} cm^{-2} formed with B_2H_6 reaction at 180 °C on Si(100) surface. Inset shows reflection high energy electron diffraction (RHEED) pattern taken from the top surface of the film. The depth profile was determined by determined by the repetition of XPS measurement and subnanometer wet etching.

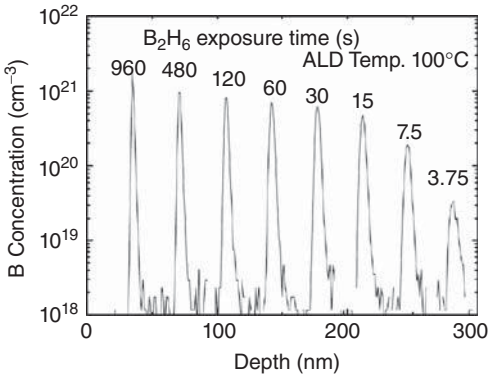

Figure 4.12 Depth profile of B peaks in Ge at different B_2H_6 exposure time at 100 °C measured by secondary ion mass spectrometry (SIMS). B_2H_6 exposure is performed on hydrogen-free Ge surface [25].

than those on tensile-strained Si, respectively, in other words, substitutional B concentration is higher in the compressive-strained Si, compared with that in the unstrained or tensile-strained Si. These results indicate suppression of B clustering due to low temperature processing as well as enhanced generation of substitutional B due to compressive strain. The data in Figure 4.4a including Ge without B-doped Si support the above consideration.

SIMS results of B atomic layer doping in Ge epitaxial growth on Si(100) by reduced pressure CVD are shown in Figure 4.12 [25]. The atomic layer doping process was performed on a hydrogen free surface at 100 °C. Very steep B profiles (<1 nm/decade) and peak concentration above 10^{21} cm^{-3} were observed with saturation for higher exposure time. This saturation is visible at low temperature only. At temperatures between 200 and 400 °C there is no saturation resulting in very high B dose indicating B clustering.

4.3.2
Phosphorus Atomic-Layer Doping in $Si_{1-x}Ge_x$ Epitaxial Growth

4.3.2.1 Surface Reaction of PH_3 on $Si_{1-x}Ge_x$(100)

By PH_3 exposure on $Si_{1-x}Ge_x$(100) [26, 27], the atomic amount of P layer formed on the surface depends on the PH_3 exposure temperature (Figure 4.13). The PH_3 reaction is suppressed on the hydrogen-terminated Si and Ge surfaces, but PH_3 is adsorbed dissociatively on the hydrogen-free Si and Ge surfaces at 300 and 200 °C, respectively. As a result, the P atomic amount on the surface tends to saturate below one atomic layer. It was reported that the saturation P coverage is 1/4 of the number of the Si surface atoms (6.8×10^{14} cm^{-2}) at 300 °C, because the dissociative adsorption of PH_3 consumes four surface sites [28]. It was also reported that the P coverage becomes lower under high pressure of H_2 [8] because of the adsorption of hydrogen even at 350 °C. However, in the present case, the P atomic amount by the PH_3 exposure to the hydrogen-free Si surface is about

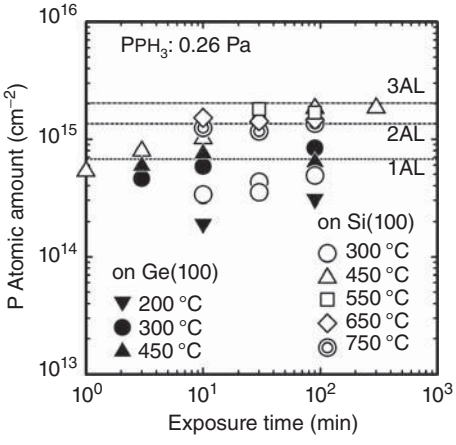

Figure 4.13 PH_3 exposure temperature dependence of the P atomic amount on Si(100) and on Ge(100), obtained by XPS.

$5 \times 10^{14}\,cm^{-2}$, which is higher than the reported value. It should be noted that the present PH_3 partial pressure is three or four orders of magnitude higher than in the report [28]. On the Ge surface at 300–450 °C, the P atomic amount tends to saturate to about one atomic layer. On the Si surface at 450–750 °C, the P atomic amount tends to saturate to about two or three atomic layers. Looking at Figure 4.13 in more detail, it can be observed that the P atomic amount is about one atomic layer in early stage.

In the case of the P desorption from the Si surface at 650 °C, the P atomic amount of the sample kept in H_2 approached one atomic layer from about two atomic layers, and the P desorption rate is faster than that in Ar. In H_k at 450 °C, a slight desorption of P was observed. Therefore, it is concluded that the P desorption is caused not only by the thermal desorption [28] but also by the reduction due to hydrogen. In the case of the Ge surface, thermal desorption and reduction due to hydrogen were also observed even at 450 °C, where the P atomic amount goes close to zero, but not at 300 °C. These results suggest that the single-atomic layer of P bonded to Si(100) and Ge(100) surface has thermal stability at 650 and 300 °C, respectively. On the other hand, looking at the effective segregation coefficient for B, P, and C inside $Si_{1-x}Ge_x(100)$ film shown in Table 4.3, it can be observed that the value of P is the lowest than that of B and C and the values at Ge–Ge and Si–Ge sites are lower than that at Si–Si site. This predicts that P atoms segregate easily at the grown Ge surface. It was reported that the segregation of Sb increases growth temperature and Ge fraction [29].

4.3.2.2 $Si_{1-x}Ge_x$ Epitaxial Growth over P Atomic Layer Already-Formed on the (100) Surface

In the case of Si growth on the (100) surface with P atomic amount of $2 \times 10^{15}\,cm^{-2}$ at a SiH_4 partial pressure of 6 Pa at 500 °C [30], surface P atomic amount decreases with increasing SiH_4 exposure time without Si deposition. When the P atomic

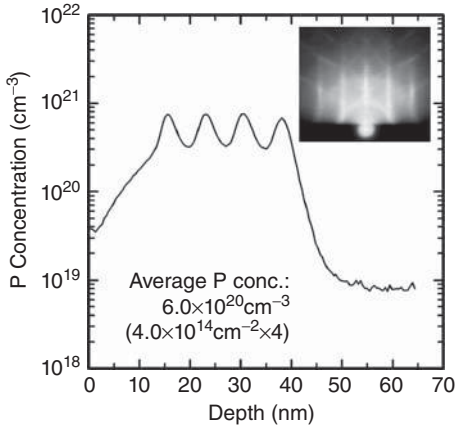

Figure 4.14 Depth profile of the P concentration in the four-layers of P doped epitaxial Si film measured by SIMS. Atomic amount of adsorbed P is $1.4 \times 10^{15}\,cm^{-2}$ for each layer. For subsequent Si growth, the SiH_4 partial pressure is 220 Pa and the temperature 450 °C.

amount decreases below single atomic layer caused by SiH_4 reaction, Si growth occurs, and P atoms segregate onto the surface.

At a rather low temperature of 450 °C and a rather high SiH_4 partial pressure of 220 Pa, heavy atomic-layer doping of P during Si epitaxial growth was achieved with average P concentration of above $6 \times 10^{20}\,cm^{-3}$ and 7 nm thick spacers (Figure 4.14) [31] and it was speculated that about $1.5 \times 10^{14}\,cm^{-2}$ P atoms were incorporated at the initial position [30] although the tailing toward surface is also observed and a part of the P atoms segregate or desorb during Si growth. In this

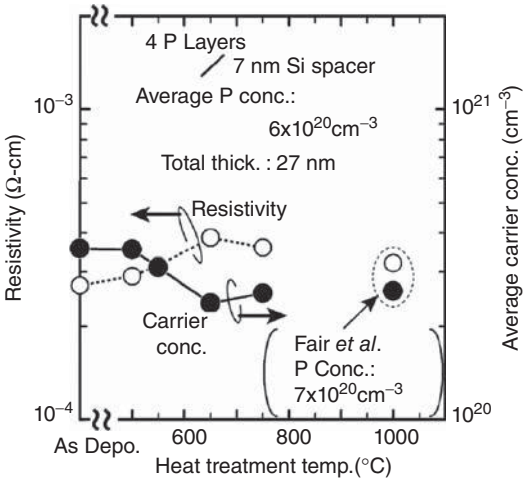

Figure 4.15 Heat-treatment temperature dependence of the carrier concentration and the resistivity of the P doped epitaxial Si films. The film was made in the same batch with the sample shown in Figure 4.14. Heat treatment time is 60 min.

case, Si deposition rate may be enhanced by Si_2H_6 produced from SiH_4. As shown in Figure 4.15, average carrier concentration reaches as high as $3.6 \times 10^{20}\,cm^{-3}$ and the resistivity as low as $2.7 \times 10^{-4}\,\Omega$-cm. By heat treatment above 550 °C, the carrier concentration decreases and the resistivity increases, and they become close to those of the P-doped Si film [32] formed by P diffusion at 1000 °C. Because the electrically inactive P atoms such as P clustering are formed by the heat treatment, the higher activity of P for the as-deposited films is expected to be out of thermal equilibrium. Using this atomic-layer doping technique, a very low contact resistivity of about $5 \times 10^{-8}\,\Omega$-cm^2 between Ti and the Si film has been obtained [33].

By Si cap layer growth using Si_2H_6 instead of SiH_4, $4 \times 10^{14}\,cm^{-2}$ P atoms were almost confined in a Si region of 2 nm thickness [27]. But, to achieve abrupt doping profiles at the heterointerface, the P surface segregation has to be effectively suppressed. Depth profiles of P atomic amount for the $Si/P/Si_{0.3}Ge_{0.7}$ on unstrained Si(100) and about 0.5% tensile-strained SOI are shown in Figure 4.16

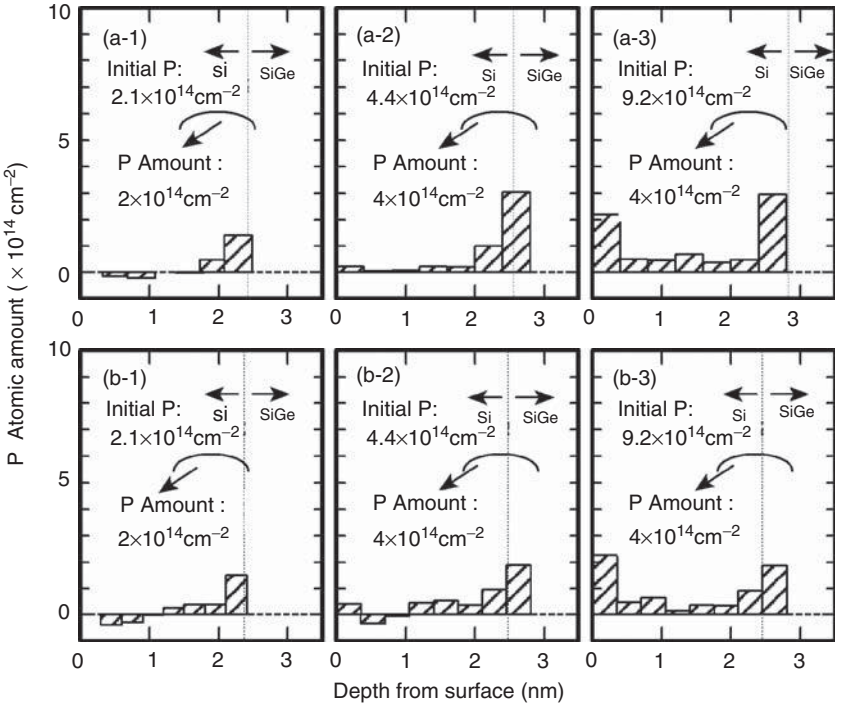

Figure 4.16 Depth profiles of P for $Si/P/Si_{0.3}Ge_{0.7}$ on unstrained Si(100) (upper) and about 0.5% tensile-strained SOI (lower). Initial P atomic amount was about (a-1)(b-1) 2.1×10^{14}, (a-2)(b-2) 4.4×10^{14}, and (a-3)(b-3) $9.2 \times 10^{14}\,cm^{-2}$. Si cap layer was deposited at 450 °C at Si_2H_6 partial pressure of 20 Pa. Interface depths was estimated from decay characteristics of Ge 3d XPS intensity. Because the P atomic amount was calculated by combination of XPS measurement and wet chemical etching of subnanometer-thick Si layer, there are negative values due to experimental error.

[34, 18]. If the initial P atomic amount is below about $2 \times 10^{14}\,cm^{-2}$, it is found that the incorporated P atoms are almost confined within 1 nm around the heterointerface. Moreover, for both the $Si/P/Si_{0.3}Ge_{0.7}$ on unstrained Si(100) and on strained SOI(100), the P atom amount is nearly the same as the initial one; in other words, P surface segregation is suppressed. However, in the case of $Si/P/Si_{0.3}Ge_{0.7}$ on strained SOI(100), especially with initial P atomic amount higher than $4 \times 10^{14}\,cm^{-2}$, the maximum value of the incorporated P atom amount at around the heterointerface (about $3 \times 10^{14}\,cm^{-2}$) is smaller than that of $Si/P/Si_{0.3}Ge_{0.7}$ on unstrained Si(100) (about $4 \times 10^{14}\,cm^{-2}$). From these results, it is suggested that tensile strain in the Si substrate enhances P surface segregation and reduces the incorporated P atomic amount at around the heterointerface, although the total P atomic amount on strained SOI(100) is almost the same as that on unstrained Si. In other words, the solid solubility limit of P in Si is reduced by tensile strain. For a sample of as-deposition for the initial P atomic amount about $2 \times 10^{14}\,cm^{-2}$, it is found in Figure 4.17 that the sheet carrier concentration of the $Si/P/Si_{0.3}Ge_{0.7}$ on strained SOI(100) is lower than that on unstrained SOI(100), although total incorporated P atomic amount in the Si cap layer on strained SOI is almost the same as that on unstrained SOI. Therefore, it is considered that the strain impacts the electrical activity of P atoms in Si. Especially in the case of unstrained SOI, the sheet carrier concentration decreases slightly at 500–600 °C. At 700–800 °C, the sheet carrier concentration increases and the difference becomes smaller. This results from the decrease of maximum P concentration by P diffusion during the heat treatment.

Depth profile of P in $Si_{0.8}Ge_{0.2}(C)$ with different cap growth temperature is shown in Figure 4.18 [19, 35]. In this case, only GeH_4 partial pressure is changed to maintain Ge concentration in the cap layer at 500 °C. Even though identical P-atomic layer doping (ALD) process is performed for both P spikes, the profile

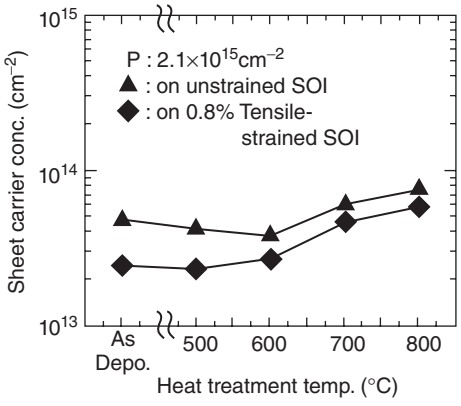

Figure 4.17 Heat-treatment temperature dependence of the sheet carrier concentration in $Si/P/Si_{0.3}Ge_{0.7}$ on unstrained Si(100) and on about 0.5% tensile-strained SOI. Initial P atomic amount was $2.1 \times 10^{14}\,cm^{-2}$.

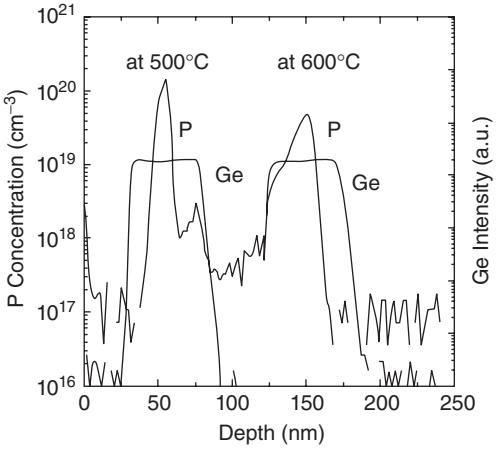

Figure 4.18 SIMS profile of P peaks in $Si_{1-x-y}Ge_xC_y$ incorporated at exposure temperature of 400 °C in N_2. SiGe:C cap deposition was performed at 600 and at 500 °C respectively [19, 35].

with 500 °C cap layer deposition is much steeper with higher peak concentration compared with 600 °C cap growth indicating lower P desorption and segregation. The P steepness could be improved from 21 to 5.1 nm/decade.

In the case of P atomic layer doping by PH_3 exposure at 300 °C on hydrogen-free Ge surface and subsequent Ge cap layer deposition at 300 °C [36], SIMS depth profile of 8 P spike with 3 nm Ge spacers shows that the average P concentration is about $3 \times 10^{20}\,cm^{-3}$ (Figure 4.19). It is confirmed that lowering the cap layer deposition temperature is needed to suppress the segregation and desorption of P [37]. Additionally, in order to suppress the impurity diffusion in Ge, introduction of Si was proposed [38].

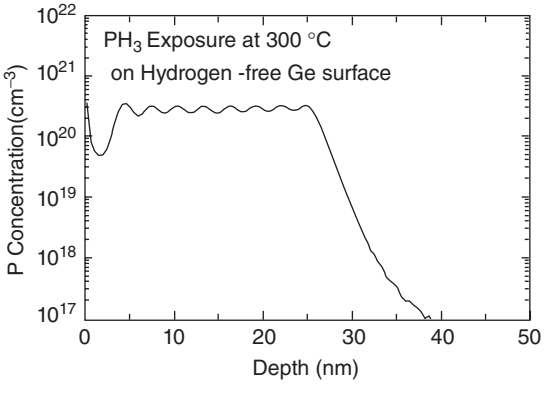

Figure 4.19 SIMS depth profile of P concentration in Ge [36]. PH_3 exposure is performed on hydrogen-free Ge surface at 300 °C. Eight identical P spikes separated by 3 nm non-doped Ge spacers are deposited.

4.3.3
Carbon Atomic-Layer Doping in $Si/Si_{1-x}Ge_x/Si(100)$ Structure

4.3.3.1 Surface Reaction of SiH_3CH_3 on $Si_{1-x}Ge_x(100)$

In the case of the CH_4 exposure on Si(100) [39], the reacted C atomic amount at the outermost surface was normalized with the product of the CH_4 pressure and the exposure time in the temperature region of 500–600 °C, and was expressed by the Langmuir-type rate equation shown in Figure 4.7 with n_T the total adsorption site density at the surface $n_T = 1.4 \times 10^{15}\,cm^{-2}$. However, at above 600 °C, the reacted C atom diffused into Si and a SiC layer was formed and, at 500 °C, the reaction rate constant of CH_4 on the Si(100) surface is $1.1 \times 10^{-5}\,Pa^{-1}\,min^{-1}$ whose value is too much lower for atomically controlled device application.

SiH_3CH_3 reacted on the Si(100) and Ge(100) surfaces even at 400–500 °C [40]. Self-limited deposition of about one monolayer SiH_3CH_3 is found at 400 and 450 °C, but the deposition at 500 °C increases continuously with the exposure time as shown in Figure 4.20. Nevertheless, at all the temperatures, the amount of deposited Si is nearly the same as that of deposited C. On comparison with SiH_4 exposure at 450 °C, it was considered that the adsorption of SiH_3CH_3 suppresses the Ge segregation on the top surface. Fourier transform infrared spectroscopy (FTIR)/Reflection Absorption Spectroscopy (RAS) results suggest that SH_3CH_3 is adsorbed without breaking the Si–C bond on the Si(100) and Ge(100) surfaces.

4.3.3.2 $Si_{1-x}Ge_x$ Epitaxial Growth over C Atomic Layer Already Formed on the (100) Surface

In order to obtain atomic-order abrupt heterointerface, it is essential to suppress dopant diffusion as well as the intermixing between Si and Ge at

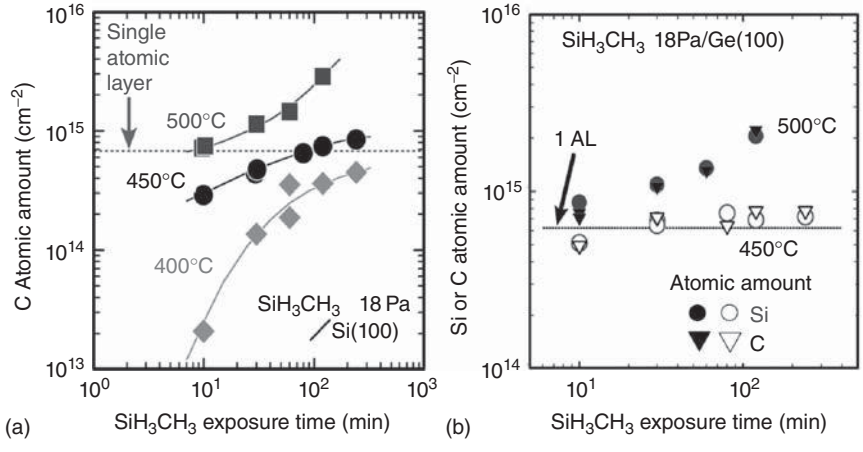

Figure 4.20 SiH_3CH_3 exposure time dependence of (a) the C atomic amount on Si(100) and (b) the Si and C atomic amounts on Ge(100) at various substrate temperatures. The SiH_3CH_3 partial pressure is 18 Pa.

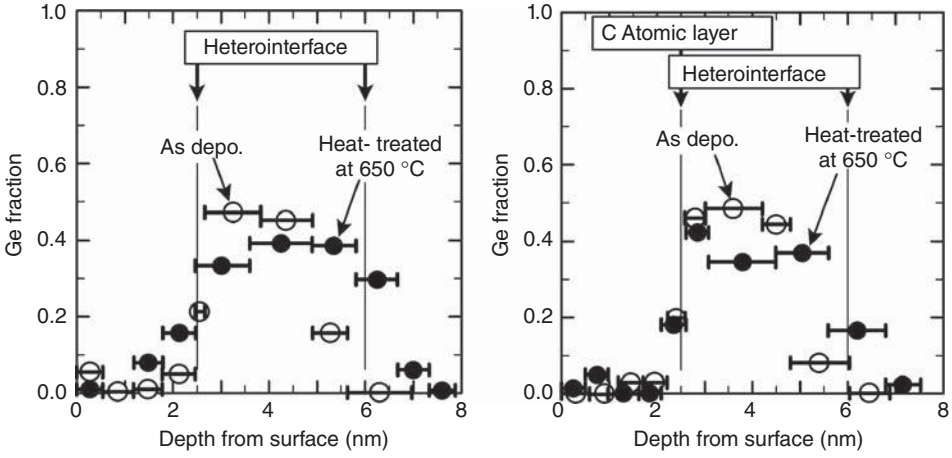

Figure 4.21 Depth profiles of Ge fraction in Si cap layer/$Si_{1-x}Ge_x$/Si(100) heterostructure (a) without and (b) with heavy C atomic-layer doping at the heterointerface between a Si cap layer and a $Si_{1-x}Ge_x$ layer before (as-deposited) and after heat treatment at 650 °C for 3 h.

Si/$Si_{1-x}Ge_x$/Si heterointerface. It was reported that C introduction into the heterostructures is effective to suppress B and P diffusions [41, 42]. By heavy C atomic-layer doping, the intermixing between Si and Ge at the heterointerface was effectively suppressed as shown in Figure 4.21 [43, 44]. From UV Raman scattering measurement results [44], the influence of C atomic-layer doping on the strain relaxation and the intermixing between Si and Ge for thin and thick $Si_{0.55}Ge_{0.45}$ cap layer on Si(100) is compared with the values for fully strained and fully relaxed $Si_{1-x}Ge_x$ films [45] as shown in Figure 4.22. For 40 nm thick $Si_{0.55}Ge_{0.45}$ cap layer, the reduction of strain amount is enhanced by C atomic-layer doping and becomes larger after the heat treatment although the Ge fraction of 0.45 was scarcely changed. For 4 nm thick $Si_{0.55}Ge_{0.45}$ cap layer with C atomic-layer doping, Ge fraction of 0.45, and strain amount are scarcely reduced by the heat treatment. For 4 nm thick $Si_{0.55}Ge_{0.45}$ cap layer without C atomic-layer doping, the Raman shift is scarcely changed with the heat treatment. In this case, by the intermixing between Si and Ge, the cap layer thickness increases and Ge fraction is reduced in the cap layer, and as a result the strain comes to be relaxed. The strain relaxation and the reduction of Ge fraction contribute to decreasing and increasing of Raman shift, respectively. This compensation explains the behavior of the Raman shift.

These results suggest that the heavy C atomic-layer doping suppresses strain relaxation as well as intermixing between Si and Ge at the $Si_{1x}Ge_x$/Si heterointerface especially for the heterostructure composed of nanometers-order thick films.

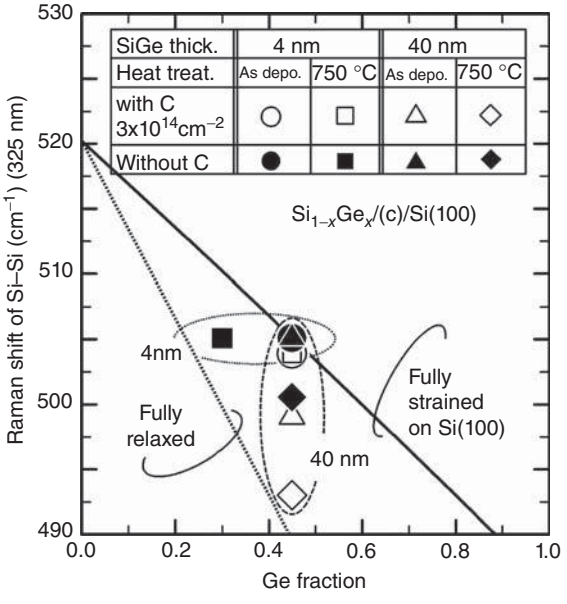

Figure 4.22 Ge fraction dependence of Raman shift of Si–Si vibration mode peak in the cap layer for 4 and 40 nm thick $Si_{1-x}Ge_x$ cap layer/Si(100) heterostructures with and without C atomic-layer doping before (as-deposited) and after heat treatment at 750 °C for 3 h. Initial Ge fraction is about 0.45. Solid and dashed lines are the values for fully strained and fully relaxed $Si_{1-x}Ge_x$ films, respectively.

4.4 Conclusion and Future Trends

In situ heavily doped $Si_{1-x}Ge_x$ epitaxial growth on the Si(100) surface in a SiH_4-GeH_4-dopant (PH_3, B_2H_6 or SiH_3CH_3)$-H_2$ gas mixture and atomic-layer doping of B, P, and C by atomic layer formation of B, P, and C on $Si_{1-x}Ge_x$ (100) surface and subsequent $Si_{1-x}Ge_x$ cap layer deposition are performed. The epitaxial growth, *in situ* doping, and atomic-layer formation processes are explained quantitatively based on Langmuir adsorption and reaction scheme. In order to obtain heavy doping as well as the steep impurity profile in $Si_{1-x}Ge_x$, the suppression of impurity segregation and desorption on the surface during $Si_{1-x}Ge_x$ cap layer growth can be performed by lowering the cap layer deposition temperature, and increasing the deposition rate of the cap layer over impurity atomic layer alreadyformed on the surface. These conditions are out of *in situ* doping under the thermal equilibrium. In order to perform very low temperature $Si_{1-x}Ge_x$ epitaxy, alternative precursors can be also required. For the suppression of the impurity diffusion in $Si_{1-x}Ge_x$, introduction of Si and/or C atomic layer during $Si_{1-x}Ge_x$ growth may be effective. Additionally, the increase of electrically active P atoms in Ge is expected by co-introduction together with Si

atoms. Moreover, the local strain control in $Si_{1-x}Ge_x$ may induce the increase of electrically active n-type and p-type impurity atoms.

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5
FEOL Integration of Silicon- and Germanium-Based Photonics in Bulk-Silicon, High-Performance SiGe: C-BiCMOS Processes

Lars Zimmermann, Dieter Knoll, and Bernd Tillack

5.1
Introduction

The space given to Silicon photonics and the widespread attention at major conferences in optical communications in recent years are clear indicators of the acknowledgment of the strategic importance of this technology. A major reason behind this interest is that near future optical transport applications have their specific requirements on optical data formats, as shown schematically in Figure 5.1. The continuing growth of traffic and the need for efficient and secure systems demand higher order modulation formats, leading to more complex constellations and therefore higher complexity of transmitters and receivers. It is general consensus that the next generation transport network scenarios will necessitate photonic integration, and Silicon photonics is a major photonic integration technology. However, Silicon photonic integration is not limited to the integration of photonic devices.

Photonic–electronic integration is highly desirable in modern communication systems where digital signal processing (DSP) is deployed in order to compensate for signal distortions caused by fiber optical transmission effects. By moving photonic functionality to the electronic domain (e.g., dispersion compensation), system cost can be reduced considerably and systems can be built more flexibly. DSP in optical communication systems rests on highly complex ASICs (application specific integrated circuits) that are typically fabricated in advanced complementary metal oxide semiconductor (CMOS) processes (<45 nm). Owing to CMOS scaling such ASICs have a low operating voltage and current driving capability, limiting their application in driving photonics. It is therefore highly desirable to develop Silicon photonic devices integrated with driving or read-out electronics plus a built-in electronic interface matching advanced CMOS. This would considerably reduce efforts in sub-system design and packaging by eliminating the need to integrate bespoke high-speed drivers and amplifiers. In terms of circuit design, such drivers and interfaces are an attractive application for high-performance BiCMOS technologies.

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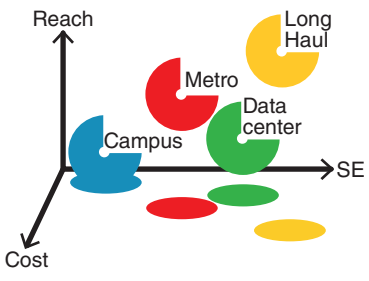

(a)

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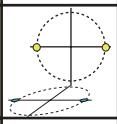
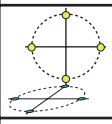
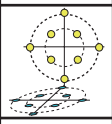
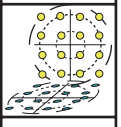
Constellation				
OSNR ++ (dB)	0	0	2	4

(b)

Figure 5.1 (a) Optical transport applications in the space of reach, cost, and spectral efficiency. (b) Examples of higher order modulation formats. (Courtesy of Wilfried Idler, Alcatel-Lucent, Bell Labs Germany.)

BiCMOS technologies also offer economic advantages. Present networks operate with per-channel data rates between 10 and 100 Gbit s^{-1}, necessitating high- speed broadband drive and receive electronics. Here, bandwidth requirements favor front-end of line (FEOL) photonic–electronic integration. In FEOL integration technology, lithographic mask area is consumed both by photonic and by electronic devices. High-speed CMOS technology below 90 nm typically makes use of advanced DUV lithography (193 nm), with considerable reticle costs. Reticle costs are lower in case of BiCMOS technologies that deploy in most cases 248 nm lithography only. Therefore, costs of a development cycle in such BiCMOS technologies are substantially lower than in an advanced CMOS process. Considering applications in transport networks, a photonic BiCMOS technology will therefore offer a cost advantage compared to highly-scaled photonic CMOS technology. This is an important asset regarding economic viability especially for small to medium scale enterprises, who will struggle with the development cost of photonic–electronic circuits in advanced CMOS technologies.

Photonic–electronic integration meets interest also outside transport network systems. Naturally, volume applications such as access networks or IPTV are excellent candidates for Silicon photonics technologies. The upgrade of existing cellular networks to meet the bandwidth demands of rapidly growing wireless communications also offers a variety of application scenarios for photonic–electronic technologies.

This chapter presents an introduction to the ongoing development of FEOL integrated photonic–electronic foundry technologies using IHP's high-performance SiGe:C BiCMOS process family SG25H, which combines a 0.25 µm CMOS core with different hetero-junction bipolar transistor (HBT) modules featuring f_T/f_{max} values up to 200 GHz [1]. The objective of this work is to add photonic modules to the baseline technology without compromising electronic performance. We shall start the chapter with our approach to merge high-performance photonics with BiCMOS technology by using local-SOI (silicon-on-insulator) technology. It follows an account of basic photonic devices

realized in the foundry. We then present the photonic integration flow, shortly discussing implications of integration in a BiCMOS baseline process, which will be followed by a section on Germanium integration, the most challenging task of all. Finally, we shall present some first results of FEOL integrated devices and provide an outlook on the technology.

5.2 Local SOI Technology

Applications demanding high-performance photonic devices necessitate the use of crystalline SOI. Photonic SOI substrates feature dimensions governed by SOI waveguide single-mode and substrate leakage conditions, similar to the typical 220 nm SOI and the 2 µm buried oxide (BOX). Such SOI parameters do not match well with the substrate parameters of present high-performance SOI–CMOS, requiring SOI thickness of only a few nanometers. Still, very first results of photonic frontend integration in an advanced CMOS technology have been presented recently [2]. Also, dense photonic–electronic integration in the FEOL of intermediate feature-size CMOS is feasible and has been shown (e.g., [3, 4]). However, photonic SOI is simply unfit for integration with a high-performance bipolar and, thus, a BiCMOS process. This is mainly for two reasons: incompatibility with collector fabrication and the higher thermal resistance compared to the bulk Silicon substrates normally used for high-performance BiCMOS or bipolar processes.

To reconcile the different substrate requirements for photonic and electronic devices, we developed the so-called local-SOI approach for a novel photonic BiCMOS process. We start with an SOI substrate with dimensions of BOX and of SOI layer optimized solely for photonic application, without any regard to BiCMOS requirements. Then SOI layer and BOX are removed locally by a sequence of RIE and wet etch steps from those wafer or chip areas foreseen for BiCMOS device fabrication. Etched areas are then re-filled by selective Silicon epitaxy and planarized by chemical mechanical polishing (CMP). The schematic process flow is depicted in Figure 5.2.

The fabrication of local-SOI substrates requires some process optimization. Figure 5.3 shows a SEM (scanning electron microscope) image of the transition area between an SOI region of the original photonic SOI substrate and a reconstructed bulk Silicon region. Two intermediate fabrication states are depicted: the wafer after selective Silicon epitaxy (Figure 5.3a), and the wafer after Silicon CMP (Figure 5.3b). The local height difference (step) between local-SOI and bulk-regions can be reduced to approximately 50 nm.

We investigated the device yield of the BiCMOS baseline on reconstructed bulk Silicon regions of local-SOI substrates. For this investigation, we used photonic SOI wafers with SOI thickness of 220 nm and a BOX layer of 2 µm. The local-SOI areas were generated according to a checkerboard pattern (see Figure 5.4) on

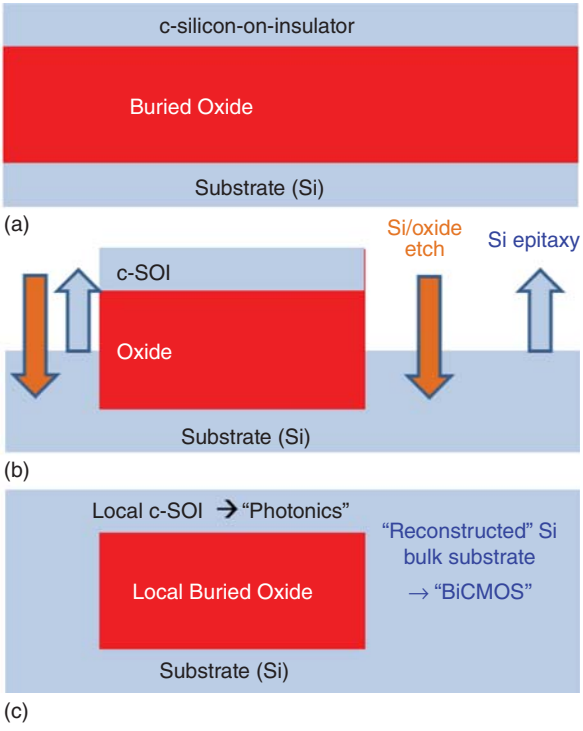


Figure 5.2 Sketch of the process flow for the fabrication of local SOI substrates. (a) Constituting photonic SOI substrate, (b) local back etch and regrowth from the silicon bulk substrate, and (c) local-SOI after silicon epitaxy and CMP.

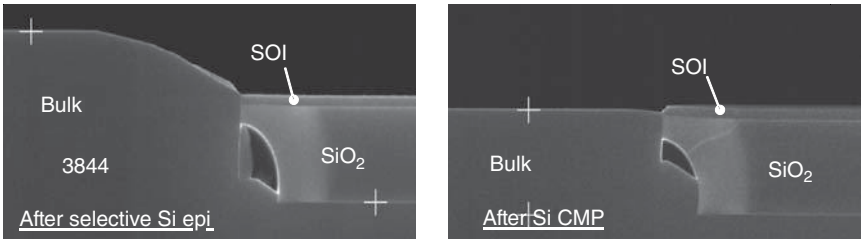


Figure 5.3 SEM images of cross-sections during the fabrication of a local-SOI substrate. Area after silicon selective epitaxy (a) and after CMP (b).

the entire wafer (i.e., always leaving a local SOI area with four neighbor areas of bulk Silicon and vice versa). SOI and BOX were locally removed from rectangular shaped areas big enough to include all the process control monitor structures and BiCMOS yield monitors typically used in the baseline process. Then, Silicon selective epitaxy and CMP were applied to form bulk Silicon regions between the remaining SOI islands. The area ratio between SOI and bulk Si regions was about

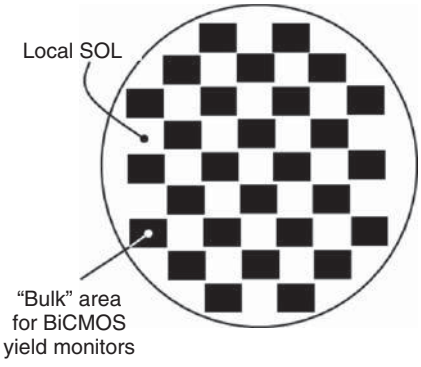


Figure 5.4 Checkerboard test pattern for the analysis of BiCMOS baseline yield on local-SOI substrates.

Table 5.1 BiCMOS yield monitor behavior: bulk versus local-SOI.

BiCMOS substrate type	Typical wafer yield (%)		
	4k HBT arrays	Low-leakage gate combs (w/total gate width of ~50 cm)	
		Gate–gate	Gate–substrate
Bulk (baseline)	>95	>99	>99
Local-SOI	90	99	97

1 : 1. After CMP and applying a careful cleaning procedure to ensure good surface quality, the normal baseline fabrication flow was carried out.

To evaluate the BiCMOS device yield data, we focus on some of our most sensitive BiCMOS yield monitors: Arrays with several thousands SiGe:C HBTs in parallel, a gate comb with a total gate width of about 50 cm, and a 1 Mbit SRAM. Table 5.1 compares yield numbers of 4k HBT arrays and gate combs obtained on wafers with local-SOI structure with the typical baseline yield data from bulk wafers.

Figure 5.5 compares the SRAM yield behavior and the behavior of even bigger, 12k HBT arrays. Despite some small differences between the baseline values and local-SOI figures, the results demonstrate that the local-SOI approach is suited to integrate high-performance BiCMOS with photonic SOI substrates.

Obviously, the model experiments with checkerboard pattern presented so far examined local-SOI, bulk, and SOI-to-bulk dimensions which were much greater than those one would apply for a real circuit fabrication. However, we could meanwhile confirm the yield data of Table 5.1 also under use of realistic design rules.

5.3
Passive Silicon Waveguide Technology

Photonic functionality in Silicon photonic technologies rests on SOI waveguide technology. SOI strip waveguides can be shrunk down to sub-micrometer

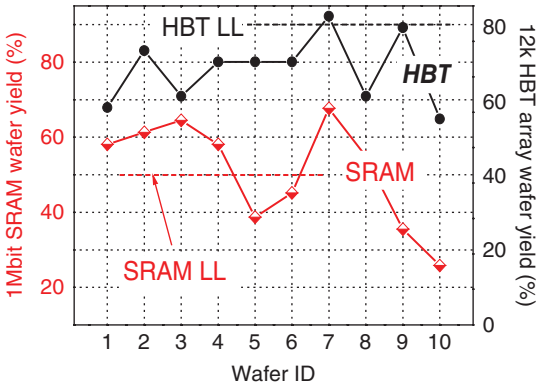


Figure 5.5 1 Mbit SRAM and 12k SiGe:C HBT array yield behavior on local-SOI substrates versus the bulk BiCMOS lower limits (LL) for these yield monitors.

cross-section but still maintain strong confinement of light, which enables designs with very small waveguide bends. At telecommunication wavelengths (around 1550 nm), experimental results have shown that strip waveguides (etched down to the BOX) with a height of around 220 nm and width of around 0.5 µm exhibit negligible bending loss for bends with radius down to only a few micrometers [5], leading to the highest possible integration density using SOI waveguides. However, such photonic nanowires also have disadvantages. A key figure of merit in PICs (photonic integrated circuits) is linear waveguide loss, which depends mainly on the interaction between the optical mode and the waveguide sidewall roughness. The large refractive index contrast between the Silicon core and the surrounding oxide cladding significantly increases this scattering loss [6]. It is difficult to reliably fabricate photonic nanowires with losses much below 2 dB cm^{-1} using deep UV lithography, especially if waveguide technology is to be compatible with integration in an electronic technology.

Nanostrip waveguides were fabricated on 200 mm SOI wafers with a 2000 nm BOX layer and 220 nm slightly P-doped crystalline silicon layer on top. Two layers of silicon nitride and thermal oxide were deposited as the hardmask for the subsequent etching of waveguides. The wafer was then coated with photo-resist and exposed by 248 nm deep-UV scanner. After development and etching, the pattern was transferred to the hardmask and the waveguide was etched down to the BOX layer. The thickness of the hardmask and the recipes of each etching step have been optimized to minimize the sidewall roughness. Cutback measurements were performed at a wavelength of 1550 nm. The measurement is depicted in Figure 5.6, showing linear loss of about 2 dB cm^{-1}. Measurements from different wafers and designs show similar loss values. The intercept of the vertical axis reveals the coupling loss. In the cut-back measurement, light was coupled in and out of the waveguide through a standard single-mode-fiber via a standard 1D grating coupler. Coupling loss of these standard gratings is typically 5 ± 0.5 dB.

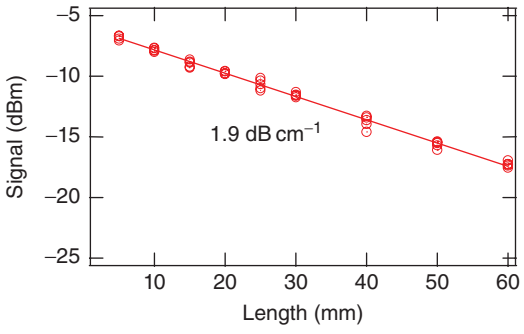


Figure 5.6 Typical cut-back graph showing linear waveguide loss at 1550 nm. Waveguide dimensions were $w = 480$ nm, $h = 220$ nm.

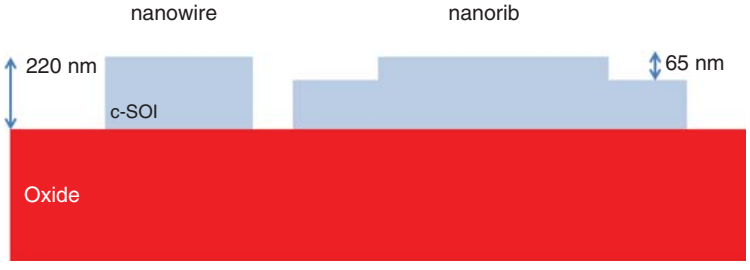


Figure 5.7 Two SOI waveguide families for integration in IHP BiCMOS, nanowires allowing for tight bends and nanoribs with low linear loss.

Linear loss of photonic nanowires is still high compared to lower index contrast waveguide technologies. This becomes noticeable in delay interferometer structures where photonic nanowires can introduce significant imbalance. Also, photonic routing on the die can introduce additional loss due to signal paths of several millimeters length. Linear waveguide loss considerably below 1 dB cm^{-1} is desirable. Linear loss of Silicon nanowaveguides can be reduced by using shallow etched waveguides of larger width [7]. In order to minimize waveguide loss we introduced an additional family of waveguides that are realized by a shallow etch forming nanorib waveguides. The two waveguide families are depicted in Figure 5.7.

Nanorib waveguides typically exhibit loss figures almost one order of magnitude lower than nanowire waveguides. Figure 5.8 depicts an example waveguide measurement using a measurement technique different from cutback measurements. Optical frequency-domain reflectometry is becoming a more widespread characterization tool in Silicon photonics after the introduction of the measurement technique to Silicon waveguide characterization [8]. The graph shown depicts the back-reflected optical power as a function of waveguide length. The peaks at the beginning and at the end of the structure result from input and output grating coupler.

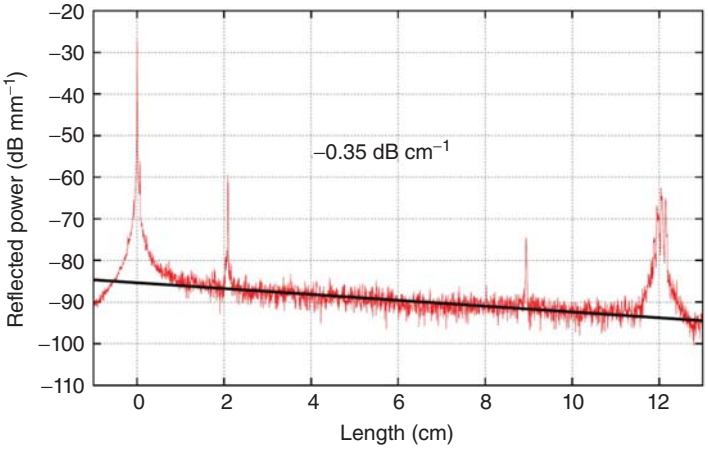


Figure 5.8 Optical frequency-domain reflectometry measurement of a 12 cm long nanorib waveguide structure. The two large peaks correspond to grating couplers. The slope between the couplers is proportional to the linear waveguide loss.

High-performance SOI waveguide technology is fundamental for realizing integrated optics with passive functionality such as filters or couplers. In addition, active functions such as o/e and e/o conversion are required to build sub-modules for photonic transmitters and receivers. Monolithic or heterogeneous integration of the laser are still in early stage development. Therefore, near-future laser integration will make use of flip-chip technology. Another option that is attractive from a system perspective is to leave the laser off chip. We therefore focus on co-integration of modulators and detectors with BiCMOS technology.

5.4 Modulator Technology

In order to modulate the phase and intensity of light in the transparency region of Silicon, we deploy a carrier dispersion effect. A change of density of free carriers in Silicon is always associated with a change of refractive index and with a change of optical absorption. Fast change of carrier density can be achieved in reverse biased PN junctions integrated with waveguides. Nanowaveguides are well suited for carrier-based modulation due to the similarity in size of the optical mode and depletion width. Two possible junction geometries are depicted in Figure 5.9. Typically, the junction profile is chosen so as to achieve maximum modulation of carrier density on the p-side because carrier dispersion is more efficient for holes within the considered doping ranges.

The change of free carrier density in a waveguide diode can be modeled using standard semiconductor device simulators (Sentaurus). Figure 5.10 shows the simulated change of hole density in a reverse biased PN diode across a waveguide for a given voltage swing $\Delta V = 5$ V.

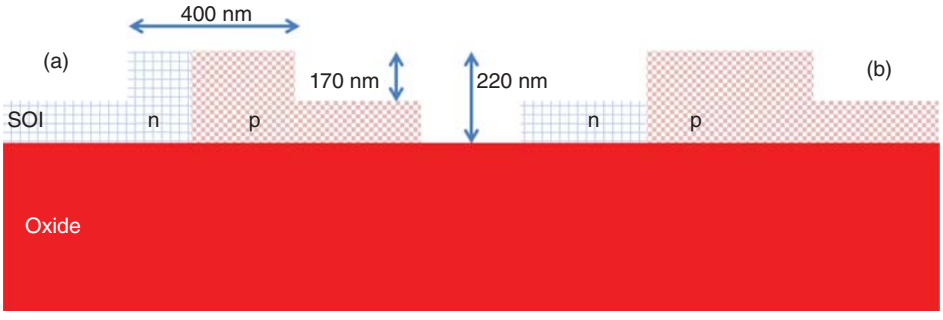


Figure 5.9 PN waveguide junction geometries for phase shifters of depletion type modulators. (a) Junction close to the center of the waveguide. (b) Junction aligned with the side of waveguide rib.

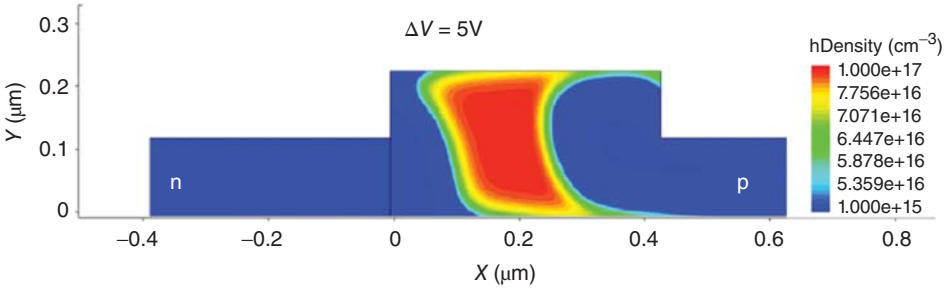


Figure 5.10 Sentaurus simulation depicting the change of hole density (Δh) in an exemplifying waveguide diode used for phase-shifting (junction type B) for a reverse voltage sweep of $\Delta V = 5$ V.

Using the overlap integral of optical mode and change of carrier distribution we can calculate phase shifter efficiency and associated free carrier loss, which is shown in Figure 5.11.

It is customary to characterize the phase shifter efficiency as a function of bias voltage. The figure of merit used to describe phase shifter efficiency is $V_\pi L$, the product of V_π (the voltage swing required to achieve a phase shift of π) and the corresponding phase shifter length L. The $V_\pi L$ product provides an efficiency characteristic normalized with respect to phase shifter length, therefore allowing for comparison between phase shifters. It turns out that $V_\pi L$ is inversely proportional to the efficiency of the phase shifter, a smaller $V_\pi L$ being preferred because it allows for shorter phase shifters or lower drive voltage and therefore lower power consumption.

Looking at Figure 5.11, there is a clear tradeoff: minimizing phase shifter absorption (i.e., optical loss of the modulator) by increasing bias voltage will decrease the phase shifting efficiency. A good decoupling of optical loss and phase shifting efficiency approaching the minimum compromise due to Kramers–Kronig relation still remains to be shown in Silicon photonic modulators.

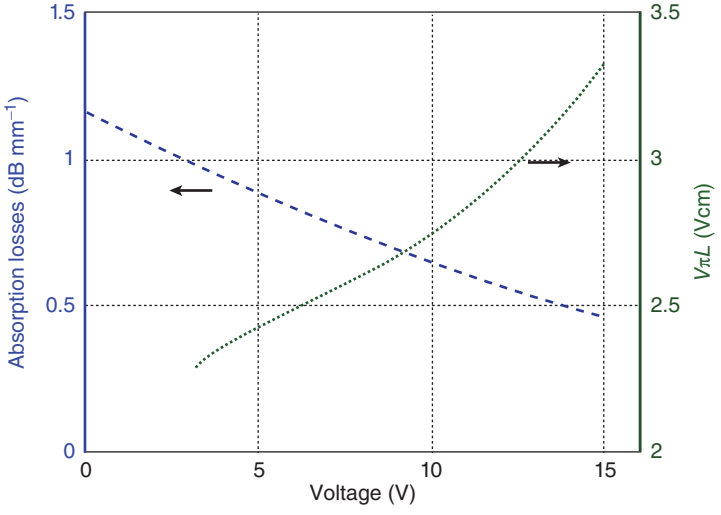


Figure 5.11 Simulated phase shifter absorption due to free carriers as function of reverse voltage for typical doping values (junction B) including linear waveguide loss of 0.2 dB mm^{-1}. The curve on the right axis shows the inverse phase shifting efficiency $V_\pi L$ as function of applied voltage.

While the focus of Silicon photonic modulator work has been on-off keying, phase-shift keying is recently receiving considerable attention as well. Within optical transport networks phase shift keying is becoming the dominant modulation scheme. Quadrature-phase shift keying has been shown by various groups using Silicon modulators; however, there is still some debate whether the nonlinear phase shift characteristic due to PN junction will allow for quadrature-amplitude modulation (QAM). In a PN junction phase-shifter there is always a correlation of phase change with amplitude change due to free carrier associated absorption. When biasing in quadrature, the absorption due to phase modulation cannot be eliminated by push-pull operation (second order nonlinearity). Hence, we expect chirp from such phase shifters.

In order to evaluate the modulation characteristics of depletion type modulators, we simulated the phase-amplitude characteristics of PN diode phase-shifters (junction A and B) in an IQ-modulator, which consists of two nested Mach–Zehnder modulators driven in push-pull. The full voltage swing is the peak-to-peak voltage Vpp. Both arms of each Mach–Zehnder are at a fixed reverse bias (Vbias). Figure 5.12 depicts the traces of the constellations realized when sweeping Vpp from zero to its maximum value. Both, the in-phase as well as the quadrature-phase components are depicted.

We observe indeed that PN junction phase shifters introduce considerable chirp, as noticeable in the departure of the lower bias trace (Vbias = 5 V) from a straight line. A phase shifter without voltage dependent loss would lead to a straight line characteristic. However, by choosing the correct biasing point and doping, chirp can be minimized. Our simulations therefore indicated that proper

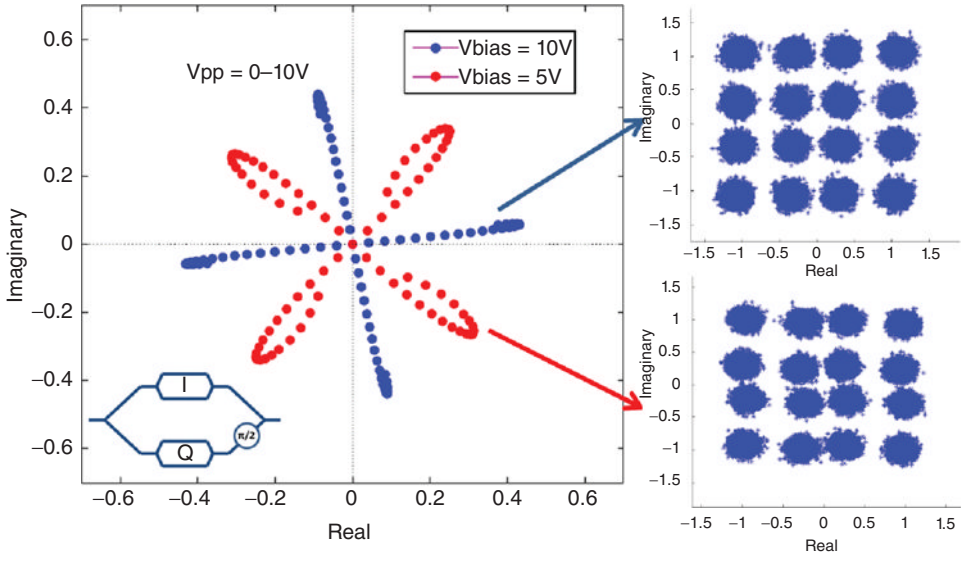


Figure 5.12 Simulated I and Q traces for a sweep of Vpp from 0 to 10 V. The arms are driven with ±0.5 × Vpp in push-pull. Deviations of the traces from the straight line reflect chirp of signal. Constellation diagrams for 16-QAM signals were generated using the two bias settings, as indicated by the arrows. The constellation deviates considerably from the ideal for the bias voltage corresponding to the less linear trace.

choice of phase shifter bias should allow for 16-QAM modulation using Silicon photonic modulators.

Various types of Silicon photonic modulators have been realized at IHP. In the following we shall present only those results on Mach–Zehnder depletion type modulators. In order to realize high-frequency operation, RF phase-shifter electrodes were designed in top-metal-2, that is, the highest metal level available in the BiCMOS BEOL, as can be seen from Figure 5.13. This way, RF loss can be reduced increasing the cutoff frequency of the device compared to RF phase shifter electrodes in thinner, low-level metals such as metal-1.

Basic performance characteristics of these modulators have been evaluated in DC as well as in high-speed operation. Here we just depict a characteristic $V_\pi L$ versus bias voltage trace (Figure 5.14), showing typical efficiency values of about 2 V cm^{-1} at a reverse bias of 4 V. Such modulators are deployed for on-off keying, as shown in the corresponding 20 Gbit s^{-1} eye-diagram in Figure 5.14.

5.5 Photonics Integration in BiCMOS Flow

In order to integrate photonics with BiCMOS electronics in the frontend-of-line, additional photonic process modules need to be added to the baseline flow. The

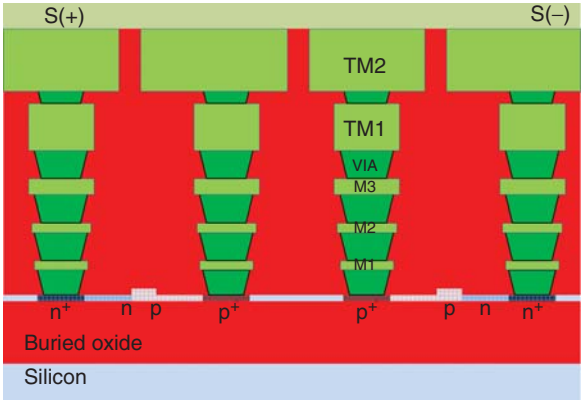


Figure 5.13 Simplified cross-section of modulator with BiCMOS backend-of-line electrodes.

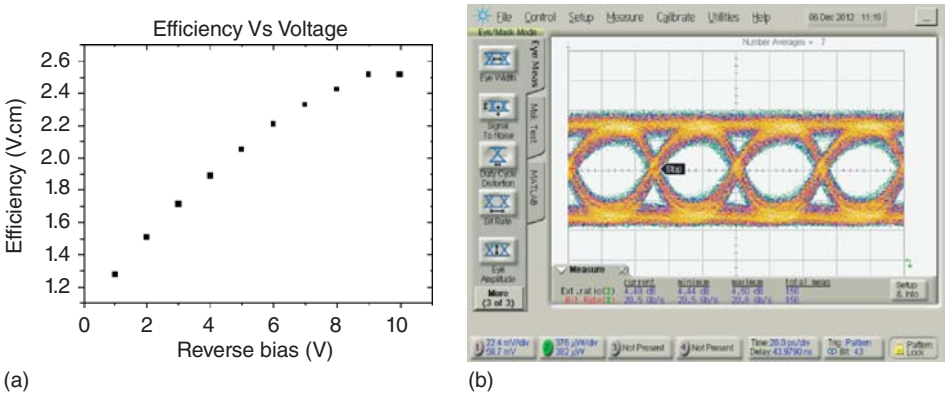


Figure 5.14 (a) $V_\pi L$ as function of applied voltage extracted from a phase shifter aligned with the edge of the waveguide. Panel (b) depicts a well-defined eye for 20 Gbit s^{-1} on-off keying (Measurements courtesy of D.J. Thomson, University Southampton).

baseline for the largest part of the integration work presented and discussed here is IHP's 0.25 µm BiCMOS process SG25H1 [1]. We think, however that the way to integrate photonic components, in particular the introduction of the local-SOI module, is not limited to this particular process but could easily be applied to many other bulk Silicon CMOS or BiCMOS processes too.

Figure 5.15 shows a global flow chart of the photonic BiCMOS process under development.

The following photonic process modules, including dedicated photo mask steps, are added to the SG25H1 BiCMOS baseline:

1) *Local SOI/WG*: A first mask is used for partitioning the wafer in SOI regions (local-SOI), foreseen for the fabrication of photonic components, and bulk Silicon regions, foreseen for the fabrication of BiCMOS devices. With a second mask, the SOI layer is etched with stop on top or even inside the BOX

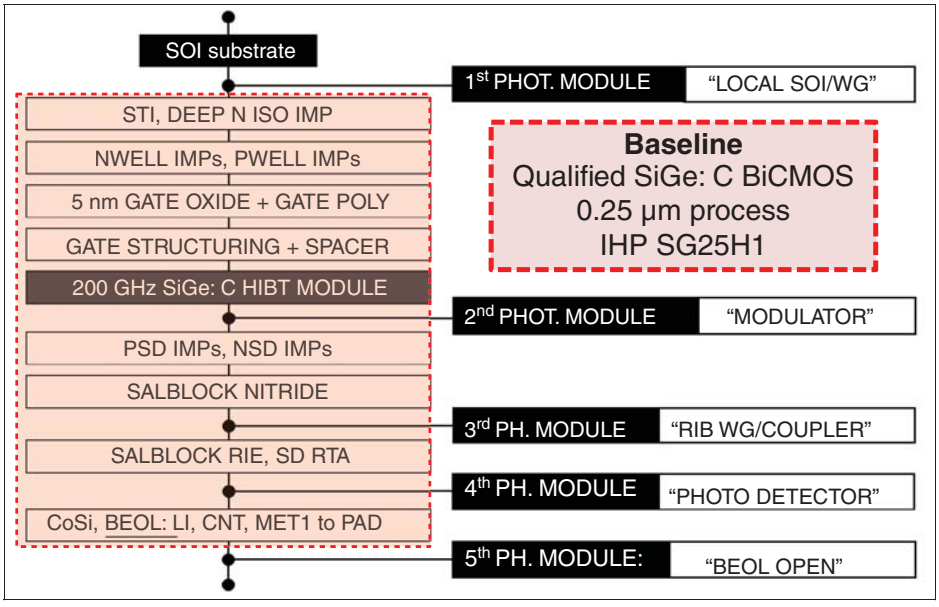


Figure 5.15 Global FEOL photonic–electronic integration flow developed at IHP. Five photonic modules are added to the BiCMOS baseline process.

to form deep etched nano waveguides that can be used for dense optical routing or as basic structures for most compact integrated optics such as splitters/combiners and wavelength selective filters.

2) *Modulator*: Implantations and an intermediate etch-depth waveguide formation are used to fabricate the frontend structure of the Silicon photonic modulator (lateral PN junction, depletion type). The electrodes are later fabricated using standard backend metallization.
3) *RIB WG/Coupler*: One mask step is applied for etching shallow trenches in the SOI layer to form low-loss waveguides simultaneously with grating coupler structures.
4) *Photo Detector*: Several photo mask steps are used to form waveguide-coupled Germanium photodiodes with lateral drift region. With a first mask a window is etched in a planarized isolator layer stack, which protects the BiCMOS devices during photodiode fabrication. Within this window the basic diode structure is formed under use of selective Germanium epitaxy. The next mask step is applied to form a pedestal on top of the detector structure to enable self-aligned contact implantations. Two masks are then used for the n-type and p-type contact implantations, respectively. Finally, the protection layer stack is removed from the BiCMOS devices with a further mask.
5) *BEOL Open*: This module can be used to remove the thick BiCMOS BEOL isolation layers from top of waveguides or grating structures, permitting access to the photonic frontend, which is required in case of photonic sensing applications.

Note that the process shares as many process steps as possible between photonic and BiCMOS device fabrication. One example is the BiCMOS shallow trench fill and planarization flow which is simultaneously used for planarizing also the waveguide structures formed with module (1). Another example is the BiCMOS CoSi contact module that is used for contacting the photodiodes as well.

5.6 Germanium Photo Detector – Process Integration Challenges

The difficulty in the integration of Germanium into the baseline process results from two fundamental facts. (i) The melting temperature of Germanium is approximately 938 °C. (ii) The lattice constant of Germanium differs from the lattice constant of Silicon by about 4%. This leads to serious tradeoffs for the integration of Germanium, as will be explained in the following.

The low melting temperature of Germanium is incompatible with the final source/drain (S/D) anneal of the frontend process. Therefore, Germanium should be introduced into the process after the final anneal. At this stage, the process is however sensitive to additional thermal load. Extra thermal input can shift electronic device parameters. This is for most cases undesirable.

On the other hand, the large lattice mismatch leads to high defect densities in the heteroepitaxial Germanium layer close to the interface with Silicon. Many ways have been devised to minimize defect density of Germanium on Silicon. Unfortunately, lowering the defect density usually goes hand in hand with increased thermal budget, for example, due to extra thermal cycling. Hence, growing Germanium after the final anneal and obtaining material with low defect density are contradictory requirements. Frontend integration of Germanium necessitates therefore a careful balancing of thermal budgets of the baseline process and of the Germanium growth.

The initial question is what Germanium material quality is required, that is, which defect density can be permitted for the applications envisaged. The photodiode parameter most sensitive to defect density is the dark current. Correlation of dark current density and threading dislocation density (TDD) has been studied [9]. Typical system specifications require dark current densities below 100 mA cm^{-2}. Thus, TDD should be around or below 10^8 cm^{-2}. A 500 nm as-grown Germanium layer exhibits defects densities well above 10^8 cm^{-2}, but defect density can be reduced by growing thicker Germanium layers. The integration in the pre-metal dielectric limits Germanium thickness to <1 μm. However, the effect of defect density reduction due to thicker Germanium material may still be used to reduce defect density in thinner Germanium layers. This is achieved by for example *insitu* etching of a thick grown Germanium layer after deposition [10]. Table 5.2 shows defect densities of Germanium layers grown on Silicon, before and after such an *insitu* etching.

Low defect density can therefore be achieved also for thin Germanium layers. Integration of Germanium photodiodes proceeds via selective epitaxy instead of

Table 5.2 Comparison of threading dislocation density (TDD) of germanium on silicon layers (full wafer deposition) before and after in-situ germanium etch.

#	Thickness (nm)		TDD (cm^{-2})
	Before etching	After etching	
(a)	500	(w/o etch)	4.3×10^8
(b)	1300	(w/o etch)	3.9×10^7
(c)	1300	**500**	$\mathbf{4.1 \times 10^7}$

The bold values indicate that low Ge thickness and low threading dislocation density are compatible.

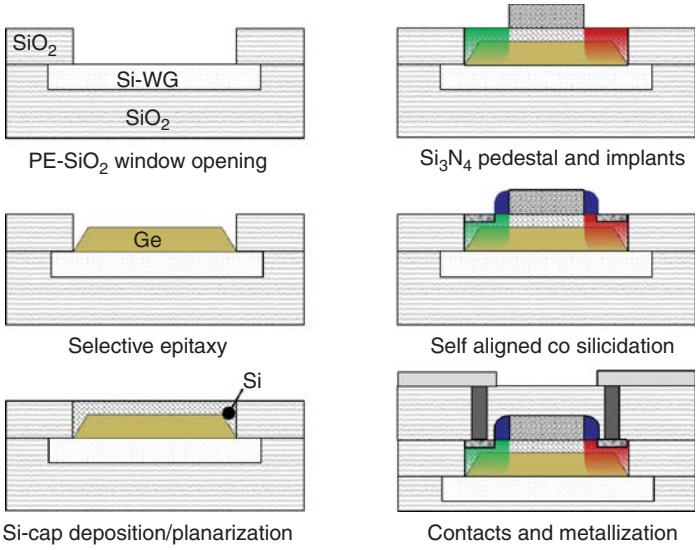


Figure 5.16 Schematic process flow for Germanium waveguide diode integration associated with photonic module (4).

full wafer growth. Selective epitaxy on comparatively small areas also aids low defect density.

In order to achieve high internal quantum efficiency and high speed operation simultaneously, absorption length and Germanium layer thickness should be decoupled. We therefore realize SOI waveguide coupled photodiodes instead of top-illuminated devices. The Germanium photodiode fabrication is depicted in the following schematic process flow (Figure 5.16). The flow shows the fabrication of PIN photodiodes with lateral PN structure, that is, a lateral drift zone. The P- and N-doped regions are in this case formed by self-aligned implantations along a silicon nitride stripe, which also defines the width of the intrinsic region. Not included are steps to thin a thicker grown Germanium layer, such as *insitu* etching. The process starts with defining selective epitaxy areas by etching trenches into

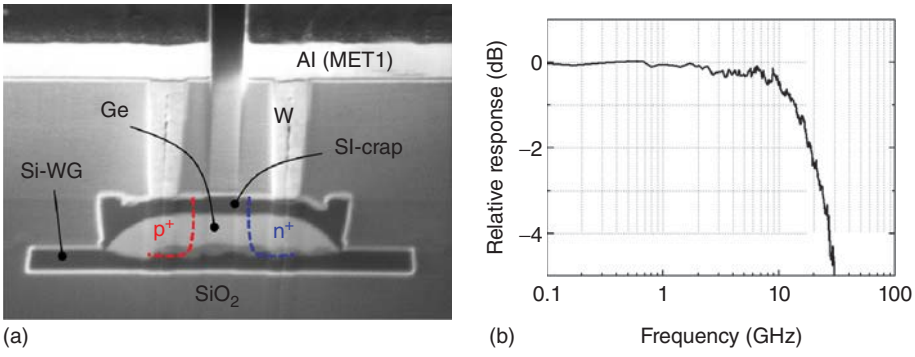


Figure 5.17 (a) SOI waveguide integrated Germanium diode. For illustration we indicated the implant areas with some diffusion under the nitride stripe. (b) The high frequency response of a lateral germanium photo detector at −2 V reverse bias, showing a 3 dB cutoff frequency >20 GHz.

the oxide on top of the SOI waveguide structures. After Germanium deposition using chemical vapor deposition a thin Silicon cap layer is added to encapsulate the Germanium and provide protection from subsequent standard cleaning procedures. The module concludes with Cobalt silicidation and the baseline contact scheme [11].

A cross-section of a lateral PIN Germanium photodiode is shown in Figure 5.17. The photodiode is seamlessly integrated into the baseline frontend, making use of the BiCMOS process, deploying silicidation and W-plugs to electrically connect to metal-1. The high frequency response of the devices shows a 3 dB cutoff frequency exceeding 20 GHz.

The dark current characteristics of the fabricated devices are governed by material quality, leading typically to dark current densities of a few 10 mA cm^{-2}. Figure 5.18 shows the IV-characteristics of a sample set of Germanium photodiodes at room temperature. The graph includes IV-curves of dark and

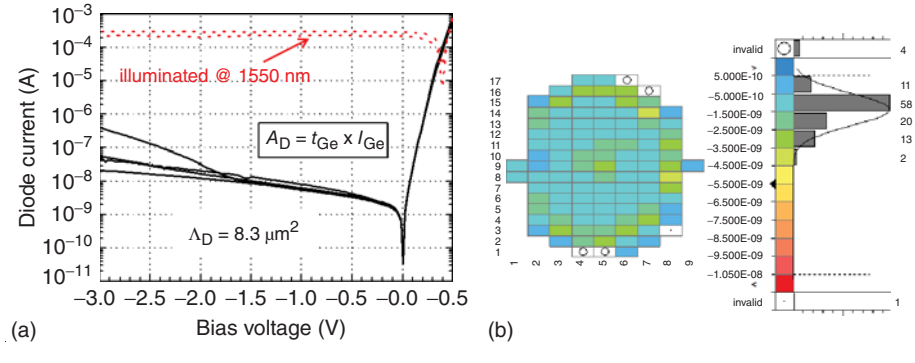


Figure 5.18 (a) IV-curves of dark and illuminated Germanium photodiodes (room temperature). Panel (b) shows a wafer map of Germanium diodes dark current values at −1 V.

Table 5.3 BiCMOS device parameters under several anneal conditions.

Anneal	HBT-R_E (Ω)	C_{MILLER} (fF/µm)		Poly-resistor R_S (Ω)
		NMOS	PMOS	
RTA (baseline)	28	0.278	0.282	301
RTA + CA	**35**	**0.325**	**0.301**	**407**
SP + CA	30.5	0.251	0.231	345
SP + PA	30.5	0.248	0.230	306

SP, spike anneal; CA, cyclic anneal; and PA, post anneal.
The bold values indicate that having the standard BiCMOS process flow plus a thermal budget related to the Ge-PD (cyclic anneal CA) yields a considerable departure of electronic device specifications from baseline.

illuminated diodes. The noticeable increase in reverse dark current with increasing bias voltage is most likely due to defect-assisted tunneling. The diodes show responsivity values of better 0.7 A W^{-1}. We also included a wafer map depicting dark current values measured on a full 200 mm wafer.

As mentioned before, Germanium diode integration needs to be concerned with the thermal budgets introduced by the Germanium growth and the resulting impact on BiCMOS parameters. We investigated the possibility of BiCMOS device parameters being compatible with the Germanium epitaxy process, including cyclic or post-epi anneals with typical temperatures in a range from 700 up to 900 °C, applied for some minutes, at the most. These anneals are typically applied to improve material quality. In our Germanium integration approach, realized with the fourth photonic module, the additional thermal budget is applied only after the final S/D anneal of the BiCMOS process, which is an rapid thermal anneal (RTA) step with a temperature of a bit more than 1000 °C. Table 5.3 shows exemplarily that adding the diode anneals to the BiCMOS flow can strongly degrade the parameters of HBTs (R_E), MOS transistors (C_{MILLER}) and poly-Si resistors (R_S). It can also be seen from Table 5.2 that dopant deactivation (R_E, R_S) and changed dopant diffusion behavior (C_{MILLER}) are issues.

Our main measure to solve these compatibility problems was not to change the conditions for Germanium epitaxy or post-epi annealing but to replace the original BiCMOS final S/D RTA by a spike anneal with much higher temperature. In tendency, the spike anneal improves dopant activation at reduced diffusion. Table 5.3 demonstrates the benefit of this measure with some room for further improvement. Replacing the original BiCMOS S/D anneal by a spike anneal with much higher T resulted in better dopant activation at reduced diffusion, which strongly helps to recover baseline parameters of CMOS and passives. However, we also need to consider bipolar transistor parameters, especially with respect to RF performance. Table 5.4 shows more detailed HBT parameters for various anneal conditions.

Table 5.4 Change of HBT DC and RF parameters, compared to the "RTA-only" baseline process, due to different annealing conditions.

Anneal	DC parameters (Δ) (%)		RF parameters (Δ) (%)	
	ΔR_{SBi}	ΔI_C (@$V_{BE} = 0.5$ V)	$\Delta f_{T,max}$	$\Delta f_{max,max}$
RTA + CA[a)]	−1.2	−6.3	+0.6	−27
SP[b)] **+ CA**[a)] **+ SP**[c)]	−3.5	−5	−2.4	−19
SP[d)] **+ CA**[a),e)]	−13	−21	−7	−18
SP[d)] **+ CA**[e),f)]	−13	−24	−6	+3

SP, spike anneal and CA, cyclic anneal.
RF device: npn 8 × 201.
a) CA after CoSi formation.
b) SP @1080 °C.
c) SP @930 °C.
d) SP @1100 °C.
e) Higher extracted base IMP-dose.
f) CA before CoSi.

We observe first that germanium diode integration, which includes some medium temperature anneals should not be done after the CoSi module. The strong HBT-f_{max} degradation for this case, which can be seen from the first three columns of Table 5.4, results mainly from an increase of the HBT base resistance, in particular from the increase of the base contact resistance. However, we also observe that a BiCMOS spike anneal, combined with germanium diode integration after that anneal, but before CoSi contact formation, even results in slightly improved f_{max} values, despite a slight degradation of f_T. This degradation stems mainly from a reduction in the collector current (I_C) due to a lower R_{SBi} which can be attributed to the better dopant activation by the spike anneal compared to anneal chains containing the original baseline RTA. However, the weak f_T degradation can easily be compensated by a bit lowering of the B doping introduced during the HBT SiGe:C base layer deposition.

In summary, we note that Germanium diode integration in high-performance BiCMOS can be achieved without the degradation of CMOS and HBT parameters.

5.7 Example Circuit – 10 Gbit s^{-1} Modulator with Driver

For a first demonstration of photonic frontend integration with BiCMOS we consider here a Silicon photonic modulator with a driver amplifier circuit. The design reflects the first learning cycle of the integrated photonic BiCMOS technology, that is, without optimization regarding footprint and performance.

The underlying SG25H3 technology allows relatively high driving voltage swings of about 5 V at speeds of 9 GHz. Details regarding the design of the

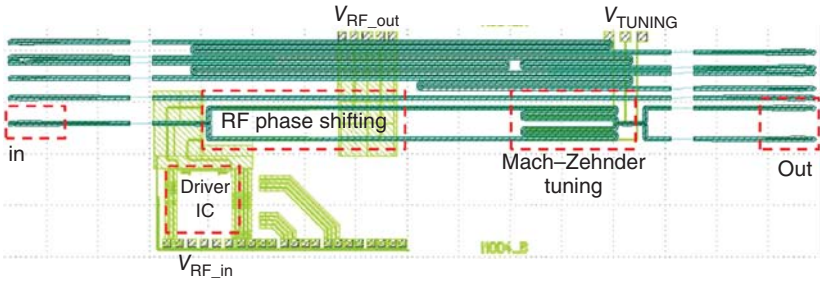
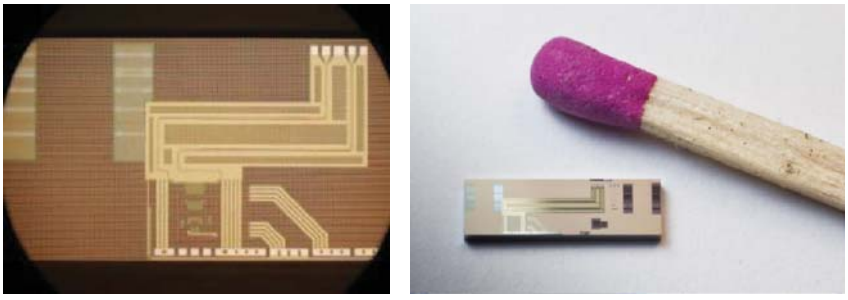


Figure 5.19 Mach–Zehnder modulator with driver layout depicting the most prominent features of the integrated device. Full size: 6 mm × 2 mm^2 (including test structures).



(a) (b)

Figure 5.20 (a) Microscope image of modulator/driver combination. (b) Example of a singled out modulator with driver IC.

amplifier circuit may be found elsewhere [12]. An overview of the integrated chip layout is shown in Figure 5.18. The Mach–Zehnder modulator requires a relatively large footprint due to low efficiency of free-carrier dispersion. The total length of the device is therefore dominated by the Mach–Zehnder interferometer. Optical input and output coupling is achieved using simple 1D grating couplers, with typical exhibit insertion loss of 5 dB per coupler for TE polarization. Figure 5.19 provides a good illustration of the typical size relations we expect for Mach–Zehnder modulator/driver combinations.

Various devices were fabricated using an IHP photonic BiCMOS testfield. Samples of realized devices are shown in Figure 5.20.

The devices were designed for 10 Gbit s^{-1} operation in push-pull configuration. Figure 5.21 depicts a sample eye diagram for 10 Gbit s^{-1} PRBS data. Clearly, the eye diagram exhibits the desired high-speed properties of the modulation such as signal integrity and low chitter. However, we also observe that amplification is required to obtain the eye pattern from the devices under test. After a first learning cycle optimization of the integration flow is required.

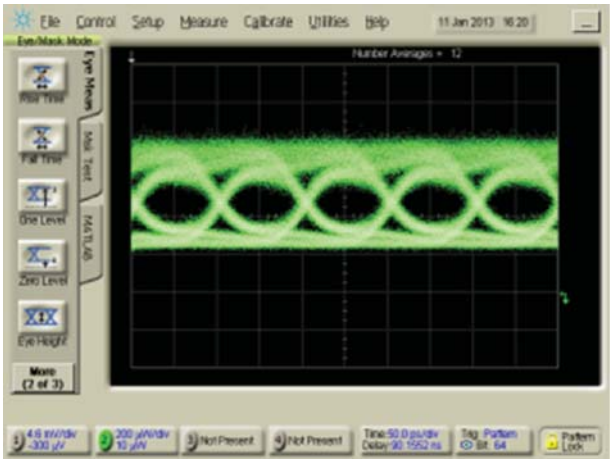


Figure 5.21 10 Gbit s^{-1} eye diagram for driver/modulator configuration. The noise level of the upper signal is due to EDFA noise. (Measurements courtesy of D.J. Thomson, University Southampton.)

5.8 Outlook

In the previous sections we have presented the current status of an ongoing development of photonic integration in the frontend of a high-performance BiCMOS technology. We could show that local-SOI technology allows for seamless integration of high-performance photonics with high-speed BiCMOS without affecting yield or performance on both sides. In addition, we have shown a viable solution to Germanium photodiode integration, despite additional thermal budget introduced by Germanium deposition and processing. We could also present first results of an integrated photonic–electronic solution, comprising a 10 Gbit s^{-1} Silicon Mach–Zehnder modulator with corresponding high-speed driving amplifier in push-pull operation. In terms of technology and HBT RF performance, 28 Gbit s^{-1} transmitters and receivers are therefore in reach. It remains to be shown that performance specifications as coming from system requirements can really be met by the photonic BiCMOS platform. This requires smart design solutions as well as improvements of the technology itself, for example, with respect to coupling efficiency. Recently, photonic BiCMOS technology has matured and additional technology demonstrators and improved device performance could be shown [13–15].

Acknowledgments

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6
Ge Condensation and Its Device Application

Shinichi Takagi

The Ge condensation method is one of the promising techniques for fabricating ultrathin Ge-On-Insulator (GOI) structures, which are quite useful for future electronic and photonic devices. In this chapter, the principle and the underlying physics of the Ge condensation technique, the properties of the GOI layers fabricated by this method, the device application of the GOI layers, and the device performance are described.

6.1
Principle of Ge Condensation and Fabrication Process

6.1.1
Basic Concept of Ge Condensation Process

The typical fabrication process of the Ge condensation method [1–4] is schematically shown in Figure 6.1. First, a standard Si-On-Insulator (SOI) substrate with a thin Si film is prepared and a SiGe film is grown on the SOI substrate. Next, this substrate is oxidized, typically in dry O_2, at high temperature and low oxidation rate. During this oxidation, Si atoms are preferentially oxidized, while Ge atoms are rejected from the oxide layer into the SiGe film, meaning that the oxidized film is SiO_2. Because the diffusion constant of Ge in Si and SiGe is quite high, Ge atoms easily diffuse from the oxide/SiGe interface and the SiGe layer toward the Si layer in the SOI substrate. On the other hand, a buried oxide layer in the SOI substrate effectively blocks the diffusion of Ge atoms through the buried SiO_2 into the supporting Si substrate. As a result, the Ge distribution becomes uniform in the remaining SiGe-On-Insulator (SGOI) layer, because of the diffusion under high oxide temperature. Simultaneously, Si atoms in the SGOI layer diffuse toward the SiO_2/SGOI interface and are consumed into SiO_2 during the oxidation at the interface. As a result, as the oxidation proceeds, the Ge content in the SGOI layer increases. Finally, when all the Si atoms included in the initial SiGe/SOI substrate are oxidized, a pure GOI film is left on the buried oxide.

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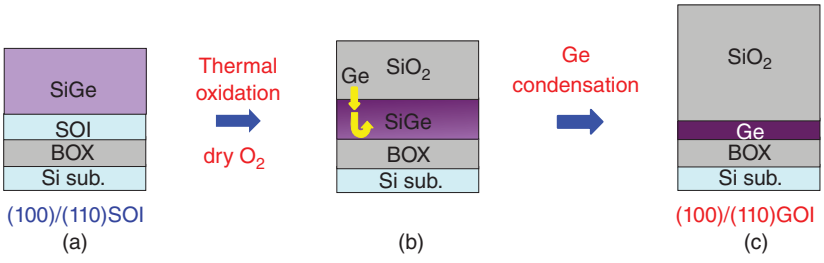

Figure 6.1 GOI fabrication process by the Ge condensation by oxidation technique. (a) SiGe layer is grown epitaxially on an SOI wafer, (b) oxidation of SGOI, and (c) Ge is condensed completely.

The change in the Ge content, x, of the SGOI layer during the Ge condensation process is often monitored in an *ex situ* way by Raman analyses. Figure 6.2 shows the change in Raman spectra for SiGe layers when increasing the oxidation time in the order of (a), (b), and (c) in the Gecondensation process [2]. A spectrum of an unstrained bulk Ge (d) is plotted as a reference. Here, the peaks labeled as I, II, III, and IV correspond to the Ge–Ge mode, Si–Ge mode, Si–Si mode in the SiGe layers, and the Si–Si mode in the Si substrate, respectively. It is confirmed that, with an increase in the oxidation time, the intensities of the Si–Ge and the Si–Si mode in the SiGe layers decrease. On the other hand, the intensity of the Ge–Ge mode increases and, finally, only the Ge–Ge mode is observed in (c), meaning that the Ge condensation is completed. The Ge content of each spectrum (a), (b), and (c) corresponds to $x = 0.45$, 0.86, and 1, respectively.

The end of the oxidation for GOI formation is usually controlled by the oxidation time. The oxidation time is adjusted so that all Si atoms included in the initial SiGe/SOI structure are consumed. The GOI layer formation is also confirmed by the fact that the Si-related peaks of II and III in the Raman spectra disappear completely, as shown in the spectrum (c) of Figure 6.2. It has been reported that this method allows us to achieve the residual Si fraction lower than 0.5% in GOI layers [2, 5]. It should be noted, however, that the GOI layer formation by the Ge condensation is not a self-limiting process. Further oxidation after completing GOI formation is known to lead to GeO_2 formation and consumption of the GOI layer [3].

Actually, this process was originally developed for fabricating a thin and relaxed SGOI template film for a strained-Si layer, regrown on the SGOI layer [1]. Figure 6.3 shows three typical applications to mobility-enhanced material channel structures by using the Ge condensation technique [6–8]. The compressively-strained SGOI layers can also be used as a channel material for pMOSFETs, because of the high hole mobility. As described later, the Ge content can be precisely controlled by the oxidation time and the compressive strain in the SGOI films can also be controlled to some extent through the initial structure and the oxidation process. Because the Ge condensation process is based on epitaxial growth and oxidation, already introduced into the standard CMOS processing,

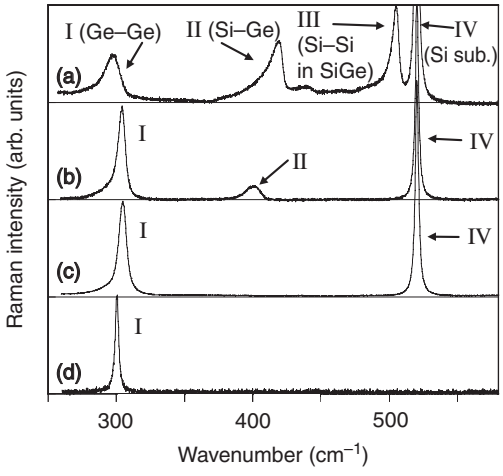

Figure 6.2 Raman spectra for SiGe layers with increasing the oxidation time in the order of (a), (b), and (c) in the Ge-condensation process. A spectrum of an unstrained bulk Ge (d) is plotted as a reference. Here, the peaks labeled as I, II, III, and IV correspond to Ge–Ge mode, Si–Ge mode, Si–Si mode in the SiGe layers, and Si–Si mode in the Si substrate, respectively. The Ge content of each spectrum (a), (b), and (c) corresponds to $x = 0.45$, 0.86, and 1, respectively.

this is one of the most realistic approaches to integrate GOI structures and devices with Si CMOS devices.

6.1.2 Critical Process Parameters

One of the most critical process parameters in the Ge condensation is the oxidation temperature [3, 9, 10]. It has been reported that higher temperature oxidation is preferred for completing the Ge condensation without cease of the oxidation of SiGe and for realizing better SGOI material quality. However, the melting temperature of SiGe significantly decreases as the Ge content increases. The melting temperature of SiGe is shown as a function of the Ge content in Figure 6.4. Thus, the oxidation temperature must be decreased gradually in order to avoid the melting. Accordingly, it is a common procedure in the Ge condensation that the oxidation temperature is decreased stepwise as the condensation proceeds, as shown in Figure 6.4. The initial oxidation temperature is often chosen to be 1200–1100 °C. On the other hand, the final temperature is usually set around 900 °C, because the melting temperature of Ge is 938 °C. The oxidation temperature midway is usually chosen as the temperature close to the melting temperature at the Ge content of each SiGe layer. This is because the higher oxidation temperature can provide better SGOI/GOI quality [9] and too low oxidation temperature sometimes ceases the condensation process [10]. These properties can be understood from the viewpoint of the balance between Ge segregation associated with

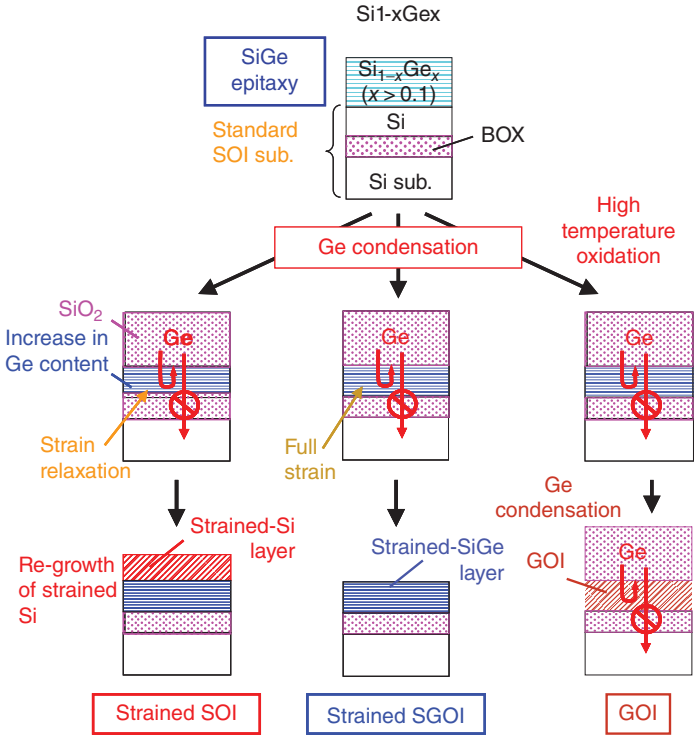

Figure 6.3 Schematic diagram of a variety of substrates including strained-SOI, strained-SGOI, and GOI, fabricated by the Ge condensation technique.

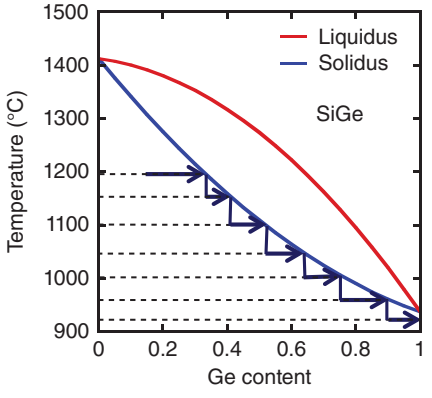

Figure 6.4 Relationship between the melting temperature of SiGe layers and the Ge content of the SiGe layers. One of the typical recipes of the oxidation temperature in the Ge condensation process is also shown.

oxidation at the MOS interfaces and Ge diffusion from the MOS interfaces toward the substrates [3, 9, 11]. At higher temperature enhancing the Ge diffusion, the pile up of Ge atoms at the MOS interfaces, induced by Ge segregation, is suppressed and the Ge profiles become more uniform, leading to continuous oxidation of SiGe and suppression of the generation of dislocations due to the less steep Ge profiles. In order to further enhance the Ge diffusion and to improve the GOI film quality, annealing processes, successively after oxidation, to be included in the Ge condensation process, have also been proposed [12–15].

6.2 GOI Film Characterization

In this section, the properties of GOI films fabricated by the Ge condensation process are described.

6.2.1 Thickness Control

When oxidation in the Ge condensation process is appropriately stopped just after oxidizing all Si atoms included in the original SiGe/SOI structure, the GOI thickness can be precisely controlled by the total amount of Ge atoms included in the original structure. Figure 6.5 shows the relation between the initial SiGe layer thickness, T_i, and the final GOI layer thickness, T_{GOI} [3]. Here, the symbols mean the experimental results. Also, the broken line means the values of $T_i \times x_i$, where x_i is the Ge content of the initial SiGe layer. A good agreement between the symbols and the broken line indicates that there is no Ge loss during the Ge condensation process and that the total amount of Ge is conserved within the SiGe layers. As a result, T_{GOI} is simply determined by the total amount of the Ge atoms, $T_i \times x_i$.

Figure 6.6 shows a typical photograph of the cross-sectional view of the GOI structures with T_{GOI} of 2 and 25 nm by transmission electron microscopy

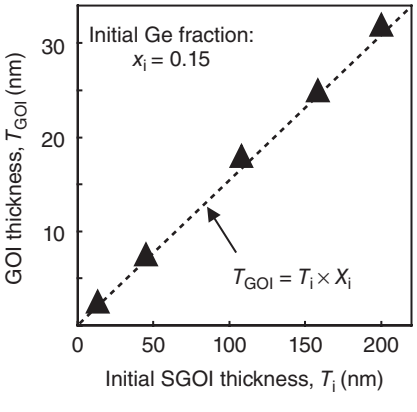

Figure 6.5 Relationship between the initial SiGe layer thickness, T_i, and the final GOI layer thickness, T_{GOI}. A broken line expresses the product of T_i and x_i, where x_i is the Ge content of the initial SiGe layer.

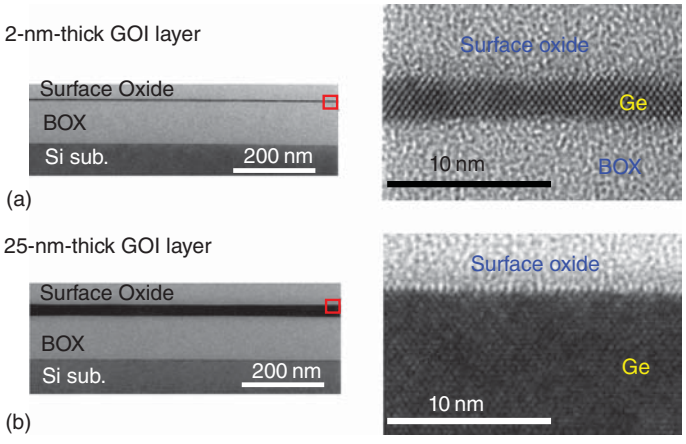

Figure 6.6 Cross-sectional TEM images of GOI layers with the thickness of (a) 2 nm and (b) 25 nm. Both layers exhibit smooth oxide interfaces as shown in the expanded images.

(TEM) [3]. The clear lattice images and the smooth Ge/SiO_2 interfaces are observed in both cases. It is confirmed from the electron beam diffraction that the crystal orientation of the Ge lattice is the same as that of the initial SOI lattice, which is (100). We have confirmed that, when a (110) SOI substrate is used as the initial one, the orientation of fabricated GOI is also (110) [16]. These results mean that the original crystal orientation is maintained throughout the condensation process.

A GOI substrate in a wafer scale has already been realized by the Ge condensation technique [3, 17–19]. Figure 6.7 shows a photograph of a 150 mm GOI wafer with an averaged Ge layer thickness of 17 nm [3, 17, 18]. One of the critical issues of the GOI substrate is the thickness variation over a whole wafer. This GOI layer thickness variation is attributable to the non-uniformity of the thickness and Ge content of the epitaxially-grown SiGe layer and the thickness of

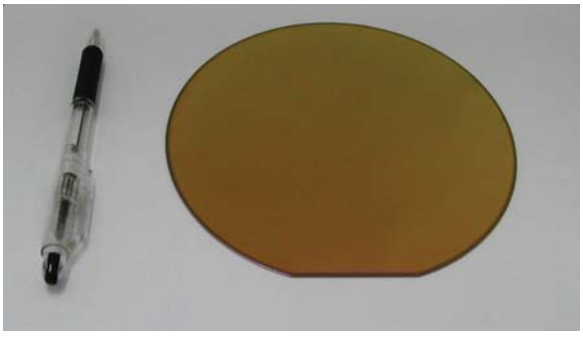

Figure 6.7 Photograph of a 150 mm GOI wafer with the averaged Ge layer thickness of 17 nm.

the initial SOI layer in a whole wafer level. Particularly, because the GOI thickness is determined by Ge atoms included in the initial structure and the GOI formation does not contain any self-limiting mechanism, the condensation process enlarges the variation. Therefore, further improvement of the uniformity of the SOI thickness, and the Ge content and the thickness of the epitaxial SiGe film is needed.

6.2.2 Residual Impurity

The purity of the GOI layer fabricated by the Ge condensation has been evaluated and analyzed by a secondary-ion-mass spectroscopy (SIMS) measurement and simulations [2, 3, 5]. An essential impurity in the GOI layer is Si. The SIMS measurements have revealed that a Si concentration in a 25-nm-thick GOI film is in the order of 10^{18} cm^{-3} [3], which is almost identical to the background level of the SIMS measurement, over the whole GOI film. The residual Si concentration is determined by the balance at the SiO_2/SiGe interface between the consumption of Si atoms due to oxidation and the diffusion of Si atoms from the deeper SGOI region toward to the interface. Thus, the high purity of the obtained GOI layer is attributed to the quite high speed of Si diffusion in SGOI layers with high Ge contents, which enables the Si selective oxidation at the MOS oxide interface until the GOI is formed. Thus, simulation results have predicted that the residual Si concentration decreases with an increase in the oxidation temperature, which enhances the Si diffusion more than the oxidation rate [3].

One of the other important impurities in SGOI is boron, because boron is often included in the initial SiGe/SOI substrate. It has been reported in the SIMS measurement for a 30-nm-thick GOI film that a B concentration in the GOI layer is $<1.4 \times 10^{15}$ cm^3 [5], which is close to the background noise level and also similar to the initial B impurity concentration of the SOI substrate. These facts mean that the B atoms are not condensed and, therefore, the impurity concentration in the GOI layers keep still low.

6.2.3 Strain Behavior

Because Si and Ge have the lattice mismatch with the amount of around 4%, a GOI layer fabricated by the Ge condensation would have 4.2% compressive strain without any lattice relaxation. It is known, however, that the GOI films are usually almost relaxed [20–24], though a small amount of compressive strain can still exist in some cases [2]. Figure 6.8 shows a typical change in the compressive strain in SGOI layers during the Ge condensation as a function of the Ge content in the SGOI layers [22]. In a lower Ge content region, the compressive strain increases in proportion to the Ge content, meaning that the strain is accumulating without any stress relaxation according to the increase in the lattice constant of SiGe.

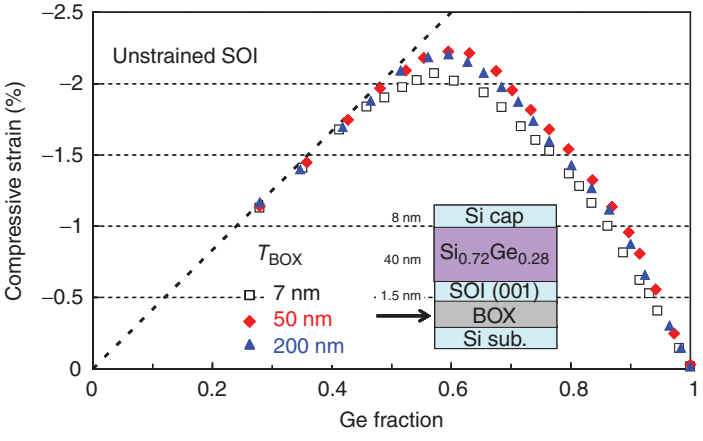

Figure 6.8 Typical change in compressive strain in SGOI layers during the Ge condensation as a function of the Ge content in the SGOI layers.

However, the strain deviates from this linear relationship with further increase in the Ge content, saturates and, finally, decreases, which is attributed to the stress relaxation.

The physical origin of this relaxation is known to be dependent on the geometrical size of the SGOI layers. When the size of SGOI is sufficiently small, the slippage between the buried oxide and the SiGe layer can contribute to the relaxation [25, 26], suggesting that the strain relaxation can occur without any crystal defect formation in an ideal case. In most cases, however, the strain relaxation is known to be caused by defect generation initiated from the accumulation of a large amount of compressive strain in the SGOI layers [20–22].

One of the main reasons for strain relaxation of the SGOI layers fabricated by the Ge condensation is the large lattice mismatch between Si and Ge. Thus, one possible way to mitigate the strain relaxation in the SGOI layers is to use a tensily-strained SOI substrate, which has a larger lattice constant than that in Si, as a starting material [23, 24, 27]. This is because the compressive strain in the SiGe layers is reduced on the strained SOI substrate with larger in-plane lattice constant than that of Si. Figure 6.9 shows the strain curve during the Ge condensation for SGOI layers on strained SOI with the tensile strain of 1.9 and 1.3 GPa and conventional unstrained SOI [27]. The dashed line and the two dotted lines indicate pseudomorphic layers on each substrate. Therefore, the deviation from the lines means strain relaxation. It is found that higher strain with an increase in the tensile strain in the starting SOI substrates is obtained at a given Ge content, meaning that the strain and the resulting lattice constant of initial substrates can effectively change the SGOI film properties such as the density of defects. However, almost no strain in pure GOI is observed, irrespective of the strain in the initial substrates, which is attributable to the behavior of easy strain relaxation in the pure GOI structure [22].

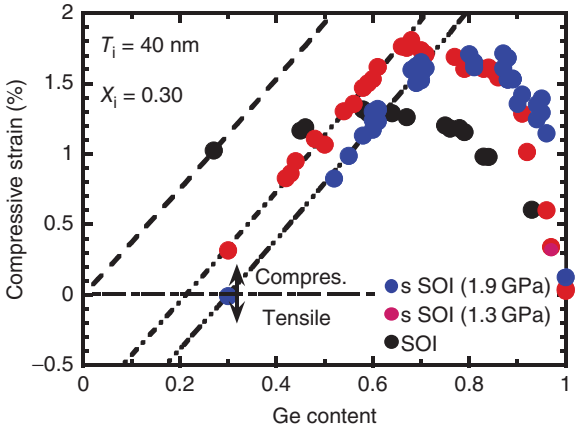

Figure 6.9 Change in compressive strain in SGOI layers during the Ge condensation on strained SOI with tensile strain of 1.9 and 1.3 GPa and conventional SOI substrates as a function of the Ge content in the SGOI layers.

6.2.4
Defects and Dislocations

It has been reported that defects in GOI layers fabricated by the Ge condensation are threading dislocations and micro-twins [20–22, 28–30]. The plan view and cross-sectional TEM images of a GOI sample are shown in Figure 6.10 [22]. Here, planar defects are shown as lines, and threading dislocations are shown as points in the plan view TEM image. It has been observed that the density of planar defects increases with an increase in the Ge content and that this increase becomes rapid around the Ge content of 0.5. Here, the structure of the main planar defects has been found to change from stacking faults to microtwins around the Ge content of 0.5. Microtwins are observed frequently in the relaxation process of strained layers [21, 31–34]. However, it has been reported that, form the viewpoint of the density, the observed microtwins cannot explain the relaxation of strain in GOI layers formed by the Ge condensation [22]. While perfect dislocations are also

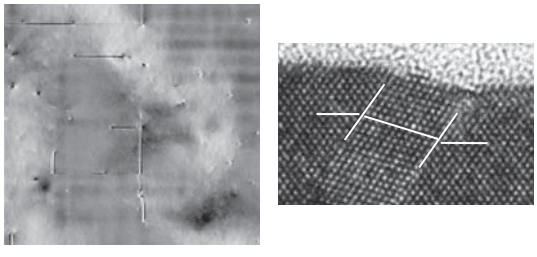

Figure 6.10 Plan view and cross-sectional TEM images of a GOI layer (a,b). Planar defects are micro-twins.

responsible for the full relaxation of the GOI layers, the detailed mechanism of the relaxation of the GOI layers has not been fully understood yet.

6.2.5 Electrical Properties

It is known that the GOI films formed by the Ge condensation contain a significant amount of free holes of typically $10^{17}-10^{18}$ cm^{-3} orders [35–37]. This hole concentration increases with an increase in the Ge content during the condensation process. Because boron concentration has been confirmed not to increase during the condensation, the physical origin of the residual holes is attributable to defects generated during the condensation. It has been reported from results of atomic force microscopy and spreading scanning resistance microscope images of a condensed GOI surface that the slip deformation generated during the condensation can induce the holes along with the slip bands [35]. However, detailed physical origins have not been fully identified yet. On the other hand, this hole generation is a critical problem from the viewpoint of the suppression of leakage current, the threshold voltage control, and the mobility reduction of MOSFETs using the GOI channels. Further reduction in hole concentration is needed for device applications.

6.3 Device Application

A Ge channel has recently stirred strong interest as a promising candidate for equivalent scaling of CMOS because of its high mobility and high compatibility with the present Si CMOS platform [38–44]. Here, MOSFETs with ultra-short channel lengths, applicable to future technology nodes, need ultrathin body structures with multi-gate electrodes, in order to suppress the short channel effects. Thus, ultra-thin body planar GOI MOSFETs and GOI MOSFETs with multi-gate electrodes such as FinFETs or nanowire MOSFETs are quite promising device structures for future technology nodes. In order to sufficiently suppress the short channel effects, it is necessary to reduce the GOI thickness roughly down to less than $L_g/4$ for planar GOI devices, $L_g/2$ for GOI FinFETs and L_g for Ge nanowire MOSFETs, where L_g is the channel length. Therefore, the GOI thickness comparable to or less than 10 nm is strongly required for these future MOSFETs with L_g of 20 nm or less. Actually, the local Ge condensation is applicable not only to the thinning but also the narrowing Ge channels, which are mandatory for advanced ultrathin body MOSFETs such as extremely-thin body planar MOSFETs, FinFETs, Tri-gate MOSFETs, and nanowire MOSFETs.

Another aspect of Ge MOSFETs is the superiority of the p-channel MOSFETs with high hole mobility over the n-channel ones, though researches on improving the performance of n-channel Ge MOSFETs have actively been conducted at present. This characteristic of Ge MOSFETs suggests that the integration of

Ge p-MOSFETs with other n-channel devices such as strained-Si n-MOSFETs or III-V n-MOSFETs on Si substrates can be one of the realistic structures for realizing advanced CMOS on the Si platform [8, 45]. For this purpose, local formation of Ge channels on Si substrates is favorable to this application.

From these viewpoints, the Ge condensation is a promising technique for fabricating advanced GOI devices. This is because the Ge condensation allows us to fabricate GOI films less than 10 nm and the local Ge condensation can form GOI regions on Si substrates locally [4, 8, 18, 23, 44–49]. In this section, the applications of the GOI layers fabricated by the Ge condensation to MOSFETs are introduced for planar and multi-gate devices.

6.3.1
Planar GOI MOSFET

MOSFETs combined with GOI structures are strongly needed for suppressing the short channel effects and the high off-current associated with the small bandgap of Ge. Actually, the p-channel MOSFETs using ultrathin GOI layers fabricated by the Ge condensation have already been reported [5, 7, 8, 15, 17, 19, 26, 29, 35, 41–56]. Long channel p-MOSFETs using 32-nm-thick GOI channels fabricated by the Ge condensation and implanted source/drain (S/D) structures have been reported with hole mobility enhancement of 3.1 against the Si universal hole mobility [17]. Figure 6.11a and b show a TEM image of GOI p-MOSFETs with a gate length (L_g) of 30 nm and the drain current (I_d) – gate voltage (V_g) characteristics, respectively [52]. Here, the 8-nm-thick Ge channels were formed by epitaxial growth on 25-nm-thick SGOI substrates with Ge content of 95%, fabricated by the

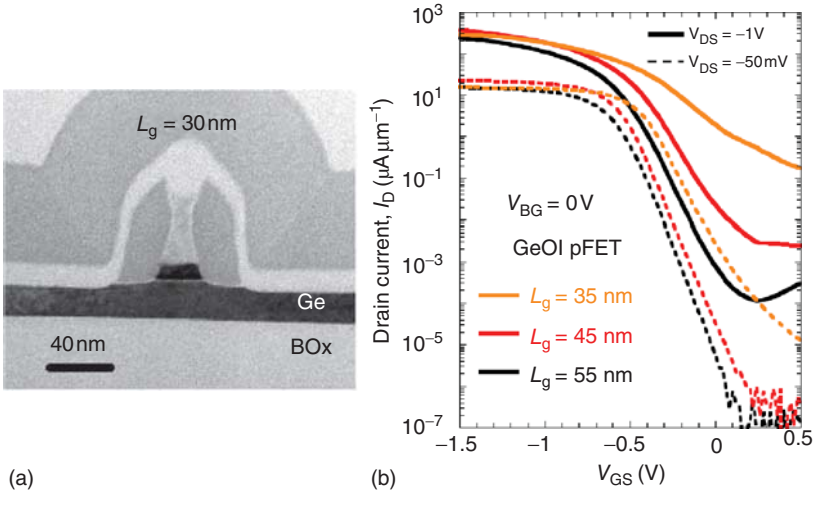

Figure 6.11 (a) Cross-sectional TEM images of a GOI p-MOSFET with physical gate length L_g = 30 nm. (b) I_d–V_g characteristics of GOI p-MOSFETs with sub-55 and 30 nm physical L_g at low (–50 mV) and high (–1 V) V_d.

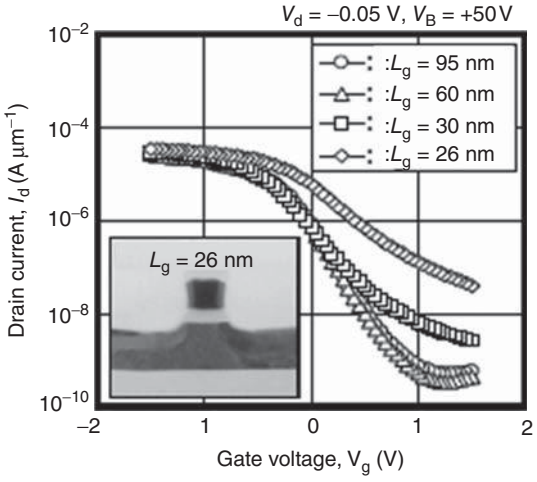

Figure 6.12 $I_d - V_g$ characteristics of GOI channel pMOSFETs with NiGe metal S/D. The large body bias (V_B) of 50 V associated with thick buried oxide of 200 nm was applied to the substrates in order to suppress the leakage current through the back interfaces.

Ge condensation. This structure has realized the significant reduction in the off-current, resulting in I_{on}/I_{off} of 5×10^5 at L_g of 50 nm. Also, I_{on} of ~200 mA mm^{-1} was reported.

Some of the GOI MOSFETs have metal S/D structures [5, 27, 30, 36, 42, 50, 52], because S/D formed by conventional ion implantation is not necessarily suitable for ultrathin body channels and the Schottky barrier height of holes between metal and Ge is quite low thanks to Fermi-level pinning of metals on Ge surfaces. 30-nm-thick GOI p-MOSFETs with PtGe and NiGe S/D have been reported [5, 50]. Figure 6.12 shows $I_d - V_g$ characteristics of GOI channel pMOSFETs with NiGe metal S/D. The MOSFET operation with L_g of down to 26 nm was observed.

While the device operations using the GOI layers have already been demonstrated, a common problem of the GOI p-MOSFETs is the large leakage current and positive shift in the threshold voltage (normally-on operation) [5, 15, 17, 19, 36, 37, 43, 44, 49–54]. This feature is caused by free hole generations in GOI channels, attributable to defect formation in GOI channels and/or GOI/buried oxide interfaces, as described in Section 6.2.5. The defect generation can be an essential problem in the Ge condensation process, because of the large mismatch in the lattice constant between Ge and starting materials, typically Si. Thus, any new engineering to further reduce the defect density is strongly needed for realizing high quality GOI MOSFETs.

On the other hand, in order to further increase the hole mobility of Ge MOSFETs, utilization of the (110) surface is known to be effective for Ge p-MOSFETs [56]. A (110)-oriented GOI structure can also be realized by Ge condensation using (110) SOI as a starting substrate [16]. The operation of the (110) GOI p-MOSFETs fabricated by this method has been reported [55, 56]. Figure 6.13a

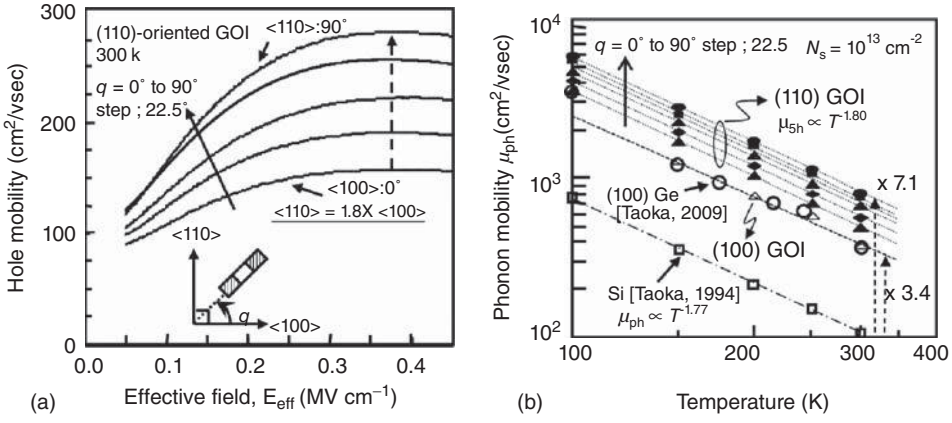

Figure 6.13 (a) Effective mobility – effective field relationship of (110)-oriented GOI p-MOSFETs at 300 K as a parameter of the channel direction. Here, the current flow direction was varied from <100> to <110> direction as a parameter of the angle tilted from <100> direction by a step of 22.5°. (b) Relationship between the extracted phonon-limited mobility of the (100)- and (110)-oriented GOI p-MOSFETs and temperature in comparison with (100)-oriented bulk Si [13] and (100)-oriented bulk Ge p-MOSFETs [15] at N_s of 1×10^{13} cm^{-2}.

shows the effective mobility (μ_{eff}) – effective field (E_{eff}) relationship of the fabricated (110)-oriented GOI p-MOSFETs at 300 K as a parameter of the channel direction [56]. It is found that the mobility is dependent on the channel direction. The highest hole mobility is obtained for the channel along the <110> direction, which is consistent with the theoretical calculation [57]. Also, the relationship between the extracted phonon-limited mobility of the (100)- and (110)-oriented GOI p-MOSFETs and temperature is shown with (100)-oriented bulk Si [58] and (100)-oriented bulk Ge p-MOSFETs [59] at surface carrier concentration (N_s) of 1×10^{13} cm^{-2} in Figure 6.13b. It is found that each phonon-limited mobility curve of GOI p-MOSFETs obeys to the temperature dependence of $T^{-1.8}$, which is close to that of Si p-MOSFETs [58], and that the amount of the mobility is enhanced, depending on the surface orientation and channel direction. These facts suggest that the mobility enhancement is attributable to the effective mass modulation. It is confirmed, as a result, that the surface/channel orientation engineering can be regarded as an effective way in improving the performance of GOI p-MOSFETs.

6.3.2 MOSFETs Using Local Ge Condensation

6.3.2.1 Planar MOSFETs

A unique feature of the Ge condensation process is its ability to realize thin GOI layers locally, which allows us to integrate GOI p-MOSFETs with other devices such as Si/strained-Si n-MOSFETs as CMOS structures. Actually, several

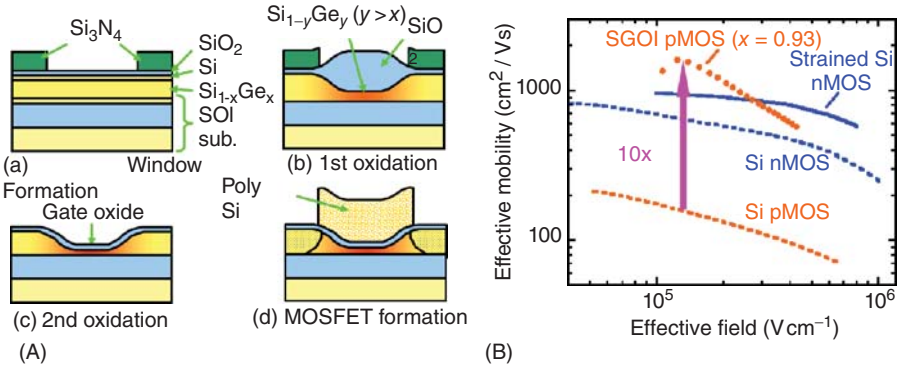

Figure 6.14 (A) Example of the local condensation process allowing us to introduce compressive strain (B) hole μ_{eff} curves as a function of E_{eff} for the SGOI p-MOSFETs with Ge content of 93%. The universal mobility in Si n- and p-MOSFETs [9] and μ_{eff} in a strained Si n-MOSFET [10] on a relaxed SiGe buffer layer are also shown.

structures of these dual CMOS structures and their fabrication processes have already been proposed and demonstrated [4, 8, 18, 23, 44, 45, 47–49]. In addition, an appropriate choice of the size of areas oxidized locally and the fabrication conditions can introduce high compressive strain in the (S)GOI channel regions without significant relaxation [25, 26, 45, 46], which is quite effective in enhancing the hole mobility.

Figure 6.14A shows an example of the local condensation processes allowing us to introduce compressive strain [46]. First, windows are opened in a SiN mask layer after the epitaxial growth of a low Ge content SiGe layer on SOI substrates. Next, local oxidation is carried out to form recessed channel regions through the Ge condensation. Then, Ge content is enhanced only below the local oxide layer by rejection of Ge atoms from the oxide layer, while the Ge fraction becomes uniform due to the inter-diffusion of Si and Ge at the high oxidation temperature. Next, the second oxidation is carried out to form gate oxide layers after the local oxide and the SiN mask layers are removed. The amount of the compressive stress has been confirmed to be 1.4% in the SGOI layers with Ge content of 93%, attributable to the small condensation areas as well as surrounding low Ge content SiGe regions. This fact indicates that a large amount of the stress can remain in almost pure GOI layers, which is in contrast to uniform condensation over large areas leading to almost full strain relaxation. Figure 6.14B shows the hole μ_{eff} curves as a function of E_{eff} for the SGOI p-MOSFETs with Ge content of 93%. It is found that a high hole mobility, which is 10 times higher than that in Si p-MOSFETs, is obtained for SGOI with Ge content of 93%, thanks to the combination of the high Ge content and the high compressive strain [8, 45, 46]. This hole mobility is comparable to the electron mobility in strained-Si n-MOSFETs, suggesting the suitability of dual CMOS composing of strained SOI nMOS/strained GOI pMOS.

Next, the examples of the CMOS integration by using the local Ge condensation are given. Figure 6.15a shows an example of the fabrication processes and the

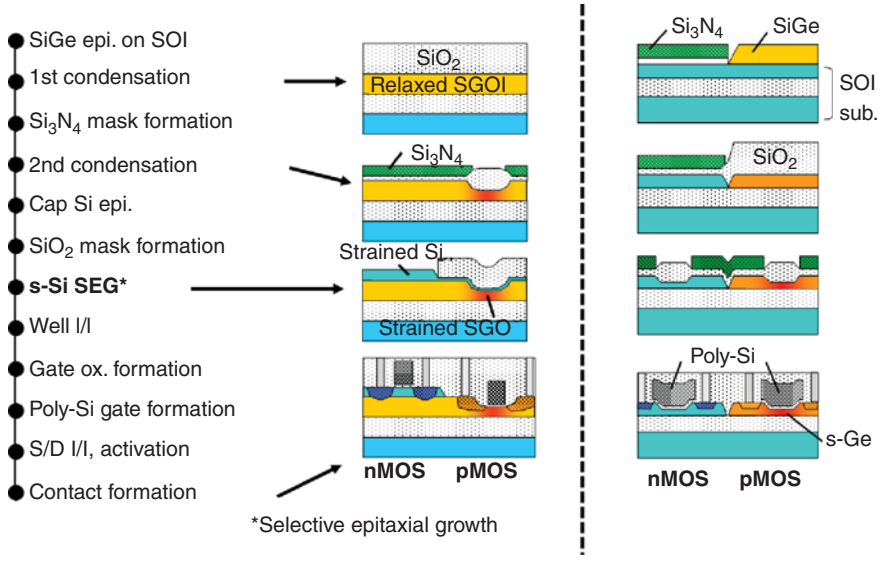

Figure 6.15 Examples of the fabrication processes and the structures of strained SOI n-MOSFET/(S)GOI p-MOSFET as dual CMOS.

structures of strained SOI n-MOSFET/(S)GOI p-MOSFET as dual CMOS, which has actually been fabricated [8, 47]. Here, a relaxed SGOI substrate formed by the first Ge condensation process is used, as seen in Figure 6.3. Strained Si layers as n-channels are selectively grown on p-well regions on the relaxed SGOI substrates. Next, strained-(S)GOI layers as p-channels are formed on the n-well regions after the second Ge condensation process. It has been reported that the fabricated CMOS devices, where the Ge content of the SGOI channels was 66%, with long channels (100 μm) exhibited electron- and hole-mobility enhancement factors of 65% and 110% at $E_{\text{eff}} = 0.5\,\text{MV cm}^{-1}$, respectively, against the universal mobility [58] in Si p- and n-MOSFETs.

An example of the fabrication processes of the strained SOI n-MOSFET/(S)GOI p-MOSFET structure is also shown in Figure 6.15b [8, 47], which is similar to those shown in Figures 6.14a and 6.15a. After Si nitride mask formation on an SOI substrate, low Ge content SiGe layers are selectively grown on the p-MOS areas. The wafer is oxidized to form recessed channel regions as the Ge condensation process, resulting in higher Ge content or pure Ge layers in the p-MOS channel regions. After that, common gate stacks are formed on n-MOS/p-MOS areas. As a result, compressively strained GOI channels can be formed in the p-MOS areas in the same manner as in Figure 6.14a. The fabricated SOI n-MOS/pure GOI p-MOS [17] have operated normally. The hole mobility enhancement factor of the GOI p-MOSFETs was 4.1 at $E_{\text{eff}} = 0.5\,\text{MV cm}^{-1}$. This enhancement factor is slightly larger than the experimentally obtained value of 3.1 for a relaxed GOI p-MOSFET [34], suggesting that the residual strain of 0.4% in the GOI layer is effective for boosting the mobility. While this low residual strain is attributable to

the tendency of strong strain relaxation in pure GOI formation, further enhancement of compressive strain through optimizing the structure and/or processing can lead to higher mobility increase.

Recently, high k/metal gate SOI n-MOS/GOI p-MOS have also been demonstrated with L_g of 270 and 160 nm by using similar fabrication processes [44, 49]. Also, if we employ strained-SOI as a starting substrate, it is expected to easily integrate tensile strain Si n-MOSFETs with compressive strain Ge p-MOSFETs in the same structure and fabrication processes [23]. As a result, the dual-channel CMOS concept utilizing local GOI channel formation by the Ge condensation can be regarded as one of the promising CMOS performance boosters. Remaining issues can be low resistance S/D formation, improvement in GOI material qualities, increase in remaining compressive strain, and demonstration of CMOS using GOI layers less than 10 nm.

6.3.2.2 Multi-gate and Nanowire MOSFETs

The local Ge condensation technique is also effective in fabricating GOI channels with narrowing the structures, which are suitable for Ge FinFETs and nanowire MOSFETs. There have already been several reports on Ge Fin and nanowire formations [36, 60–62]. Figure 6.16 shows one of typical fabrication flows of Ge Fin or nanowire formation [36]. First, narrow SGOI wires are patterned by standard anistrophic etching on an SGOI wafer. Here, the SGOI substrates can be fabricated by the standard (two-dimensional) Ge condensation technique. After that, the SGOI wires are oxidized (three-dimensional Ge condensation) again. In this process the width and height of the SGOI wires decrease, and the Ge content inside the wires increases. The advantages of this method for fabrication of Ge nano-wires are summarized as follows: (i) only the top-down and Si compatible processes are employed, (ii) the diameter and Ge content of nano-wires can be precisely controlled by the oxidation time and/or the initial wire width, and (iii) defect formation accompanied by the increase of strain during the Ge condensation could be suppressed, particularly in narrow Fins or wires, because edge-induced elastic strain relaxation is expected to take place in these small mesa structures [25, 26].

Figure 6.17a and b show top view and cross-sectional TEM pictures, respectively, of a SiGe wire structure after the three-dimensional condensation for SGOI with initial wire width of 80 nm [36]. It is confirmed that the uniform wire structure is fabricated. Also, Figure 6.17c shows the trans-conductance (g_m)–V_g characteristics with changing the Ge content during the condensation. Here, the diameter of the wires is reduced down to 130 and 40 nm for SGOI with Ge

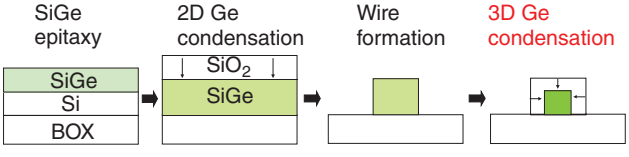

Figure 6.16 Schematic illustration of proposed fabrication procedures for Ge nano-wire. 2D and 3D Ge condensations are properly utilized.

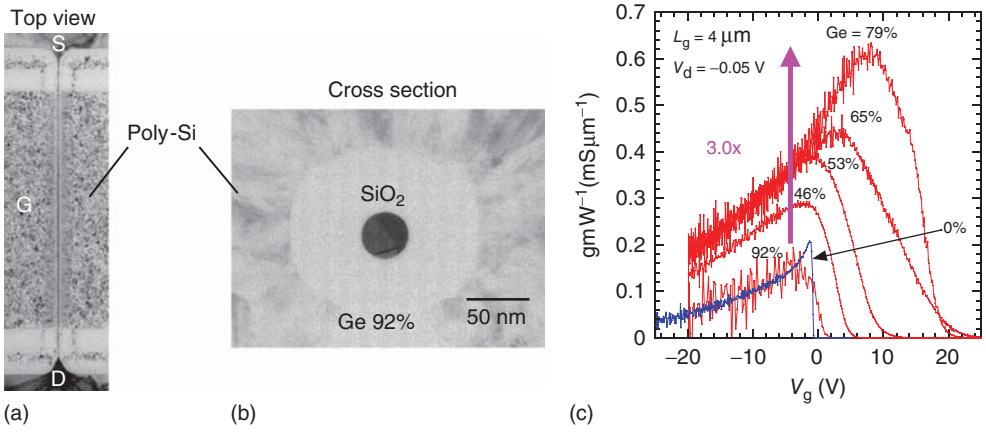

Figure 6.17 (a) Top view and (b) cross-sectional TEM pictures of a SiGe wire structure after the three-dimensional condensation. (c) Trans-conductance (g_m)–V_g characteristics with changing the Ge content during the condensation.

content of 79% and 92%, respectively. It is found that g_m increases by increasing the Ge content, although g_m significantly decreases at the Ge content of 92%. When the Ge content reaches 79%, g_m increases by a factor of 3 against the control Si device. These results indicate the effectiveness of three-dimensional Ge condensation for Ge nanowire formation with hole mobility enhancement. On the other hand, the rapid reduction in g_m in the Ge content of 92% is attributable to grain boundaries generated during the Ge condensation through non-optimized oxidation processes. The optimization of the wire structure and the process conditions is expected to provide high quality Ge nano-wire MOSFETs. As a result, the Ge condensation can be one of promising ways to form Ge nano-wire channels.

6.3.3
Stressor

SiGe alloys have also been commonly used in modern MOSFETs for logic applications as an embedded S/D material for introducing stress into channels [63–66]. It has been reported that embedded SiGe S/D regions as stressors can be formed by selective epitaxy of SiGe regions with low Ge content and successive local oxidation of the SiGe regions, which can increase the Ge content and resulting compressive strain [67, 68].

6.3.4
Photonic Devices

Ge is known to be a material for photonic devices such as photo detectors, because of the good match of the band gap with the wavelength of light used in optical fiber communications. Also, Ge is recently expected to be a Si-compatible

material for light emitting devices. Thus, GOI structures formed by the Ge condensation can be applied to those photonic devices. Actually, the integration of Ge photo-detectors with GOI MOSFETs and SGOI waveguides applicable to optical modulators, both of which were fabricated by the Ge condensation, has been reported [69, 70].

Also, a Ge fin light-emitting diode has been proposed as a monolithic light source on a Si photonics chip [71]. Actually, the Ge fins aiming at this application were fabricated by the Ge condensation of SiGe sidewalls epitaxially grown on Si fins. Here, a tensile stress was applied to the pure Ge fins by the difference of the thermal expansion coefficient with that of the surrounding oxide. The strong electroluminescence with the spectra consistent with those expected from direct recombination in Ge with the tensile stress was observed. As a result, this structure is promising for the future application of the electrically-pumped laser diodes composed of group IV materials, easily integrated with the Si CMOS platform.

6.4 Summary

In this chapter, we have reviewed the principle of the Ge condensation method, films properties of the fabricated GOI structures, and the device applications. The typical results and the current status of MOSFETs using the GOI structures as the channels have been introduced. Because the Ge channel MOSFETs have been regarded as one of the most promising and realistic technology boosters in the future nano CMOS, the Ge condensation method is strongly expected to provide a fabrication technique to selectively form high quality and ultrathin GOI structures on Si substrates. One of the most critical issues for utilizing GOI fabricated by the Ge condensation is the improvement of the material quality, particularly the reduction in the amount of the defects, the dislocations, and resulting residual free holes. Further optimizations of the fabrication technique, novel ideas to reduce the defect density, and the understanding of the generation of the defects and relation to the electrical properties are still strongly needed.

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7
Waveguide Design, Fabrication, and Active Device Integration

Koji Yamada

7.1
Introduction

Recently, various germanium (Ge) photonic devices have been developed on the silicon (Si) photonics platform, in which state-of-art Si/Ge semiconductor technology would provide us with inexpensive, highly integrated, functional photonic systems. Similarly to existing silica-based and III–V semiconductor-based photonics platforms, the silicon-based photonics platform requires optical waveguides for constructing and integrating photonic devices. For this purpose, the waveguides must have features that allow us to accommodate passive and dynamic photonic devices, such as wavelength filters and modulators based on Si and Ge. The waveguides must also be flexible enough to implement active functions, such as light emission and detection based on Ge. Furthermore, for monolithic integration of photonic and electronic devices, a very important advantage of the silicon photonics platform, the waveguides should be constructed on Si substrates or be constructed together with Si/Ge electronic devices. This requirement is also very important in integrating passive photonic and dynamic/active photonic devices with Si/Ge electronic device structures. Of course, the waveguides should guarantee a sufficiently low propagation loss and small bending radius for implementing these photonic functions on a chip, whose typical size is a few centimeters square.

These requirements are very difficult to meet with conventional waveguides. For example, the fabrication process for conventional silica-based waveguides requires high temperatures exceeding 1000 °C, which would seriously damage the electronic structure of modulators, detectors, and other electronic devices. Moreover, silica-based waveguides have a large bending radius on the order of millimeters, making it impossible to integrate photonic devices on a centimeters-square chip. Waveguides and photonic devices based on III-V compound semiconductors have geometries smaller than those in the silica-based system; however, on a Si substrate it is very difficult to epitaxially grow the high-quality III–V materials needed for the construction of practical photonic devices. The etching and other fabrication procedures are completely different from those in

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the fabrication processes for Si. Thus, a simple and natural conclusion has been derived: silicon-based waveguides are preferred over other types of waveguides for the silicon-based photonics platform.

Recently, two types of silicon waveguides have been developed: photonic wire waveguides with a submicrometer-size core and rib-type waveguides with a micrometer-size core. Ge photonic devices can be integrated with both types. The rib-type waveguide with micrometer-size core is advantageous in fabrication tolerance; however, because of its large core dimensions and large bending radius, it is neither very suitable for high-density, compact device integration nor high-speed device operation. The photonic wire waveguide has very small core dimensions and tight bends and is suitable for high-density integration and high-speed operation, though it requires severe fabrication tolerance. In optical interconnection, which is the most promising future application of photonics, high-density integration is the most important issue. In this chapter, thus, we mainly review the design and fabrication of silicon photonic wire waveguides, which has a significant potential for high-density integration. The wavelength region of interest for propagating electromagnetic waves is that from 1.2 to 1.7 μm, which is widely used in telecommunications and optical interconnection applications.

7.2 Design of Silicon Photonic Wire Waveguiding System

7.2.1 Guided Modes of Si Photonic Wire Waveguide

A schematic of the cross-sectional structure of a silicon photonic wire waveguide is shown in Figure 7.1a. The waveguide consists of a silicon core and silica-based cladding. The core size should be determined so that a single-mode condition is fulfilled. In this waveguide, the refractive index contrast between the core and cladding is as large as 40%, which allows very tight confinement of light in the waveguide core. The core size is around half of the wavelength of electromagnetic waves propagating in silicon, or a few hundred nanometers for 1310–1550-nm telecommunications-band infrared light. Generally, the core is made flat along the substrate to reduce the etching depth in practical fabrications. In many cases, the height of the core is typically half of the width, and a typical core geometry is a $400 \times 200\ \mathrm{nm}^2$ rectangle.

Figure 7.2a,b show numerically calculated effective indices n_{eff} of guided modes for 1550-nm infrared light in various core geometries [1]. The film mode matching method (FMM) was used for the calculations [2] and the indices of silicon and silica were set at 3.477 and 1.444, respectively. The mode notations are taken from Ref. [3], in which E^x and E^y modes represent the transverse electric (TE)-like and transverse magnetic (TM)-like modes, respectively. As shown in Figure 7.2a for waveguides of 200-nm silicon thickness, single-mode conditions are fulfilled when the core width is less than 460 nm for TE-like guided modes, in which the

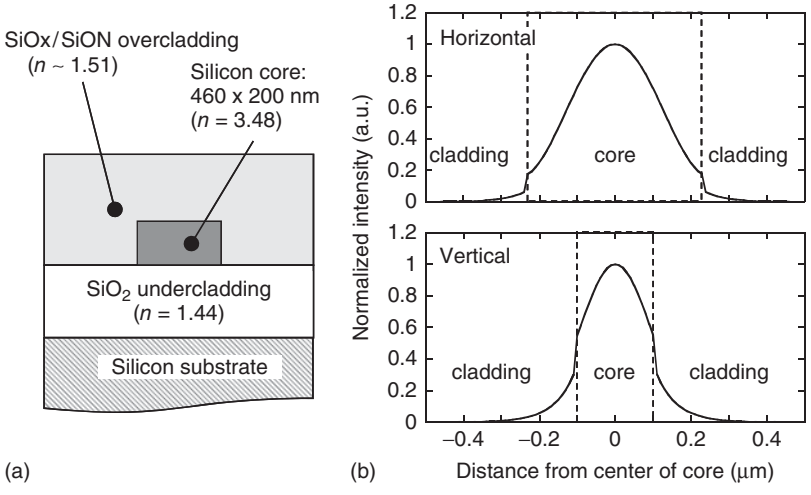

Figure 7.1 (a) Cross-sectional structure and (b) optical intensity distribution of a typical silicon photonic wire waveguide.

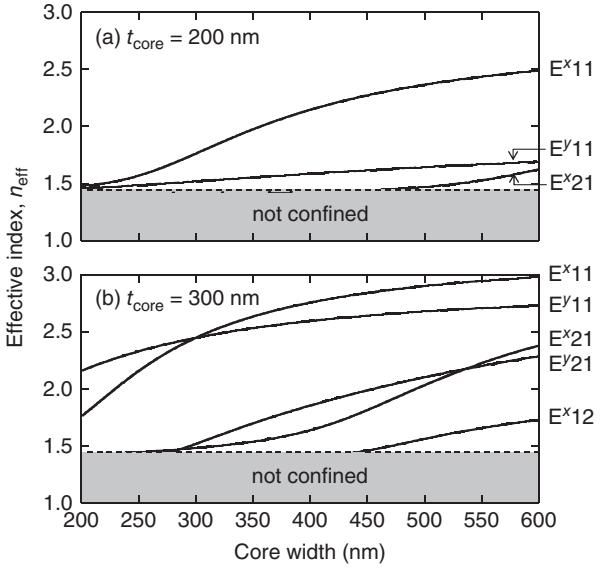

Figure 7.2 Core width dependence of effective indices of silicon photonic wire waveguides with (a) 200-nm-thick and (b) 300-nm-thick cores.

dominant electric field is parallel to the substrate. The field profile of the TE-like fundamental mode is shown in Figure 7.1b for a $460 \times 200\text{-nm}^2$ core [1]. For a TM-like mode, in which the dominant electric field is perpendicular to the substrate, the single-mode condition is fulfilled in a core larger than that for the TE-like mode. The effective indices of TE and TM fundamental modes show a large

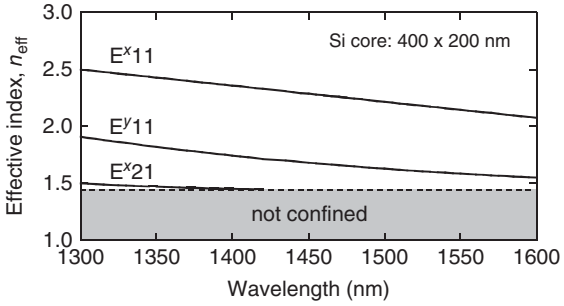

Figure 7.3 Wavelength dependence of effective indices of silicon photonic wire waveguides.

difference. In other words, the 200-nm-thick flat core produces large polarization dependence. For waveguides with 300-nm-thick silicon, silicon core widths satisfying single-mode conditions are smaller than those for 200-nm-thick silicon, as shown in Figure 7.2b. In a 300-nm^2 core, the refractive indices are identical for the TE and TM fundamental modes; that is, the polarization dependence would be eliminated.

Figure 7.3 shows the calculated wavelength dependence of the effective refractive indices for waveguides with a 400×200-nm^2 core [1]. The FMM was used for the calculations and the material dispersions of refractive indices were considered. As shown in Figure 7.3, the single-mode condition is violated in the wavelength region below 1420 nm for the TE-like mode. For the 1310-nm telecommunications wavelength band, a smaller core should therefore be used to satisfy the single-mode condition.

As shown in Figure 7.2, the effective indices of silicon photonic wire waveguides are extremely sensitive to the core's geometry. The group index n_g, which is an essential parameter in designing delay-based devices, such as optical filters, is also affected significantly by it. Figure 7.4 shows calculated group indices and their sensitivity to core width $dn_g/n_g dw$ [1]. For TE-like modes, for which most photonic functions are designed, the sensitivity is around 2×10^{-4} nm^{-1} for a 400×200-nm^2 core. For wavelength filters for dense wavelength division multiplexing, the group index should be on the order of 1×10^{-4} or less. The index restriction corresponds to a core width accuracy of 0.5 nm or less, which is essentially unattainable with current microfabrication technology. In order to reduce the sensitivity of effective indices to geometrical errors, waveguides with very wide cores have been proposed. For example, in an arrayed waveguide grating (AWG) filter, waveguides with 750×200-nm^2 cores have been used to reduce phase errors due to the variation of core width [4]. When we use a waveguide with such a wide core, however, higher order modes stimulated in bending and other asymmetric structures become a concern.

Figure 7.4 also suggests that the structural birefringence is incredibly large and that the problem of polarization dependence in a silicon photonic wire waveguide is practically unsolvable. In a waveguide with a 400×200-nm^2 core, the group

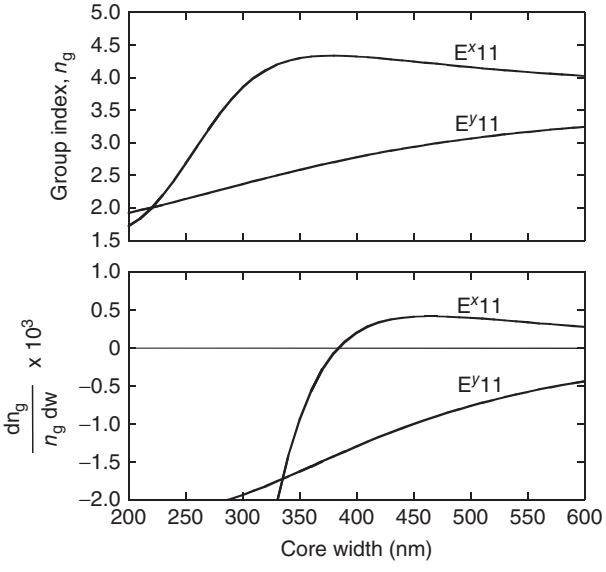

Figure 7.4 Core width dependence of group indices and their derivatives for waveguides with 200-nm-thick cores.

indices are 4.33 for the TE-like fundamental mode and 2.78 for the TM-like fundamental mode. The difference in the group indices gives a large polarization mode dispersion, which seriously limits the applicable bandwidth in high-speed data transmission. The polarization-dependent wavelength in delay-based filter devices, such as AWGs and ring resonators, would be incredibly large. A square core would not be a solution to this problem because the group index is very sensitive to core geometry. In other words, polarization diversity is necessary for eliminating the polarization dependence in photonic devices based on silicon photonic wire waveguides.

The propagation loss of photonic wire waveguides is mainly determined by scattering due to surface roughness of the core. The effect of the surface roughness on the scattering loss in dielectric waveguides has been theoretically studied and formulated by Payne and Lacey [5], and the upper bound of the scattering loss α_{max}, as given in Ref. [6], is expressed as

$$\alpha_{max} = \frac{\sigma^2 \kappa}{k_0 d^4 n_1}, \tag{7.1}$$

where σ, k_0, d, and n_1 are the root-mean square roughness, wavevector of light in a vacuum, half-width of the core, and effective index of a silicon slab with the same thickness as the core, respectively. Although κ depends on the waveguide's geometry and the statistical distribution (Gaussian, exponential, etc.) of the roughness, its value is on the order of unity for most practical waveguide geometries [5]. Thus, the scattering loss is inversely proportional to the fourth power of d. In other words, it will seriously increase in photonic wire waveguides with an ultrasmall

core. A roughness of only 5 nm, for instance, would cause a 60-dB cm^{-1} scattering loss in a 400-nm-wide core made of a 200-nm-thick silicon slab whose effective index is 2.7. To achieve a practical scattering loss of a few decibels per centimeter, the surface roughness should be about 1 nm or less.

7.2.2 External Coupling of Silicon Photonic Wire Waveguide

Since a silicon photonic wire waveguide has a very small mode profile, spot-size conversion is essential for connecting it to external circuits such as single-mode optical fibers. At present, two types of spot-size converter (SSC) have been developed: a grating coupler [7, 8] and an inverse taper coupler [9, 10]. A schematic of the grating coupler is shown in Figure 7.5. The coupler structure is a simple Si surface grating fabricated on a laterally expanded core. Although the coupling efficiency is around or less than −4 dB; its vertical coupling performance permits wafer-scale testing of photonic devices. A schematic of the inverse taper coupler is shown in Figure 7.6. The coupling efficiency of the inverse taper is as high as or over −1 dB, although it requires a rather complicated structure with a very thin taper and a second medium-index silica or polymer core. In a typical design for 1550-nm-wavelength infrared light, the tip of the taper should be ultimately reduced to less than 100 nm and the silica-based waveguide has a 3-μm^2 core with a 2.5% index contrast to the cladding [10]. In such a double-core structure, light leaking from the silicon taper is captured by a silica-based waveguide, which guarantees efficient optical coupling to external optical fibers.

Figure 7.7 shows the calculated conversion efficiencies between a silicon photonic wire waveguide with a 400×200-nm^2 core and a silica-based waveguide

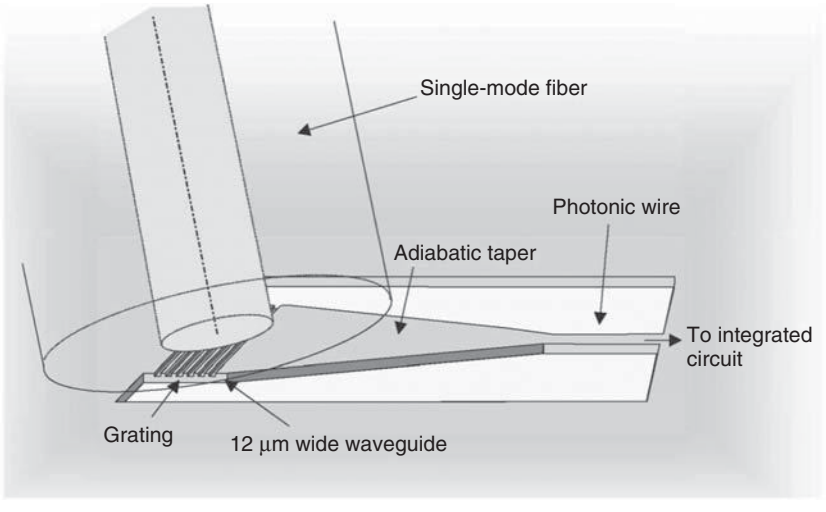

Figure 7.5 Schematic of grating coupler.

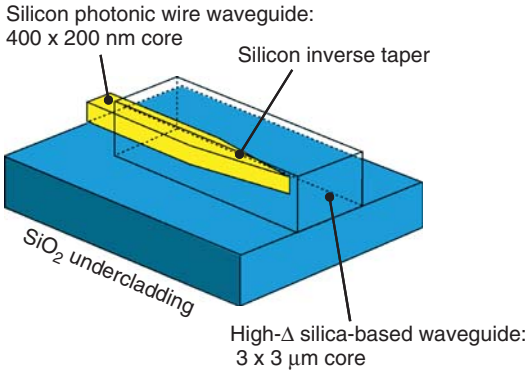

Figure 7.6 Schematic of spot size converter with an inverse taper.

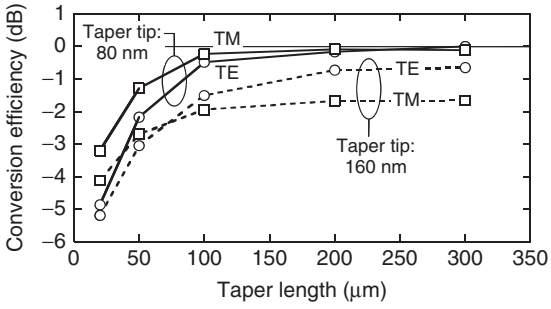

Figure 7.7 Calculated conversion efficiencies in spot size converters with various geometries.

with a 3-μm^2 core [11]. As shown in this figure, the conversion loss for a 200-μm-long taper with a 80-nm tip is around 0.1 dB for both polarizations. The coupling efficiency would be lower for a shorter and thicker taper. Because the coupling loss between a silica-based waveguide with a 3-μm^2 core and a high-numerical-aperture (NA) fiber with a 4.3-μm mode field diameter (MFD) is about 0.1 dB and the conversion loss between a high-NA fiber and an ordinary single-mode fiber can be reduced to about 0.1 dB by applying a thermally-expanded-core technology [12], a total coupling loss of less than 0.5 dB can be achieved between a photonic wire waveguide and a single-mode fiber.

7.2.3 Coupling to Ge Photonic Devices

For low-loss connection between a Si waveguide and Ge photonic devices, such as photodiodes, an evanescent coupling structure is widely used. Figure 7.8a shows a conceptual schematic of evanescent coupling. The input waveguide is a simple Si channel waveguide, whose core width is expanded toward the entrance of the

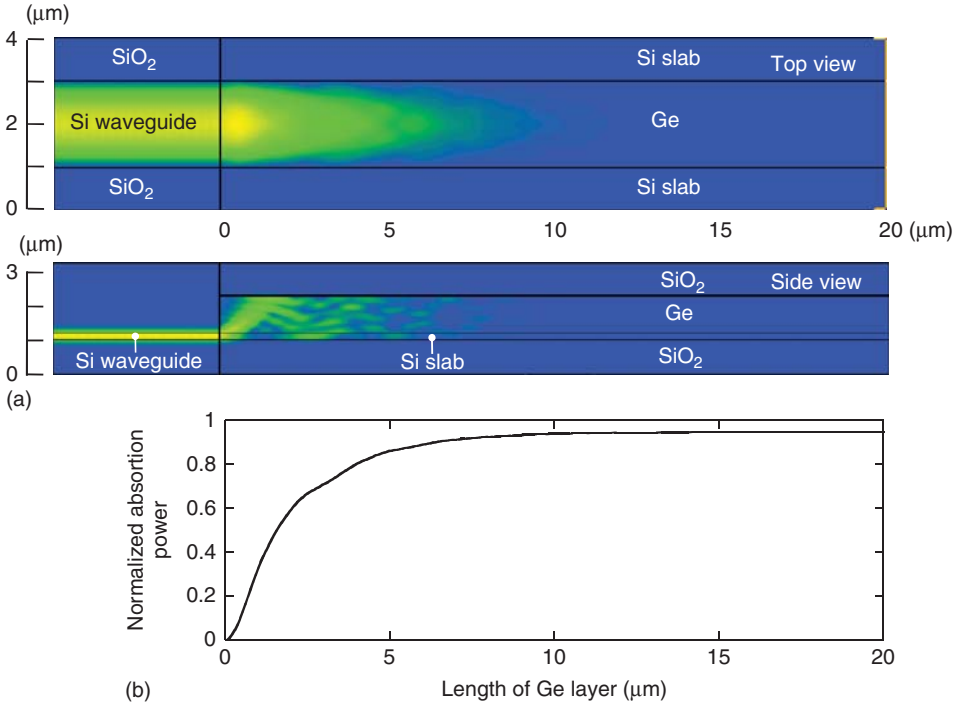

Figure 7.8 Evanescent coupling from Si waveguide to Ge photodiode. (a) Schematic of evanescent coupling structure and field intensity of propagating light. The field intensity is integrated with respect to the normal directions. (b) Calculated optical power absorbed in Ge layer.

Ge photodiode. A Ge mesa is constructed on the Si slab connected with the input waveguide. In this coupling structure, the Si waveguide and slab have the same thickness; therefore, Si waveguides and a platform for Ge devices can be easily fabricated by applying one simple etching process. The field intensity of propagating light in this structure, calculated by the eigen-mode method with a commercially available code [13], is also shown in Figure 7.8a. The wavelength of propagation light is 1.55 μm, which is widely used in telecommunications applications. Widths of the Si waveguide core and Ge mesa are assumed to be 2 μm, and thicknesses of Si core/slab and Ge mesa are 0.2 and 1 μm, respectively. The assumed refractive indices of Si and Ge are 3.478 and 4.27 and those of the SiO_2-based undercladding and overcladding are 1.44 and 1.46, respectively. The absorption coefficient of Ge is assumed to be 4600 cm^{-1}, which is significantly enhanced by applying tensile stress [14]. From the Si waveguide, light from the Si waveguide is injected under the Ge mesa. As the Ge-mesa/Si-slab structure works as a loaded waveguide, the injected light is efficiently captured into the Ge layer. Figure 7.8b shows the normalized optical power absorbed in Ge with respect to the length of the Ge mesa.

Approximately 95% of the optical power is absorbed in a 10-μm-long Ge mesa. The other 5% is scattered at the entrance of the mesa.

7.3 Fabrication

There are many variations of the fabrication process for waveguide-based Si and Ge photonic devices and they continue to be further improved and refined. In this section, a typical fabrication process is described.

7.3.1 Si Waveguide Core

A silicon photonic wire waveguide is typically fabricated as follows. First, a resist mask layer is formed on a silicon on insulator substrate. A hard mask, which is often made of SiO_2 or silicon nitride, may be added to improve etching selectivity. Next, waveguide patterns are defined by electron beam (EB) lithography or excimer laser deep ultraviolet (DUV) lithography [15], which are capable of forming 100-nm patterns. Ordinarily, EB and DUV lithography technologies are used in the fabrication of electronic circuits, for which they are optimized for patterning of straight and intersecting line patterns; therefore, no consideration has been given to curves and roughness in pattern edges. The curves and roughness in pattern edges are important factors in fabricating low-loss optical waveguides. In order to reduce propagation losses of the waveguides, for example, it is necessary to reduce the edge roughness to around 1 nm or less. This means that particular care must be taken in the data preparation for EB shots or DUV masks [16]. The writing speed of the EB lithography must also be considered in practical fabrication. For practical purposes, it is probably necessary to use EB lithography with a variable-shaped beam.

After resist development and SiO_2 etching for a hard mask, the silicon core is formed by low-pressure plasma etching with electron-cyclotron resonance (ECR) plasma or inductive coupled plasma.

7.3.2 Dynamic and Active Layers

Protecting the waveguide from environmental contamination requires an overcladding thickness of a few micrometers or more, and such a thick overcladding layer can be a serious obstacle to the fabrication of electronic device structures. Electronic structures for dynamic and active devices, such as Si modulators and Ge photodetectors, should be constructed before overcladding deposition.

For Si-based dynamic or modulation devices, which have a kind of Si p-n or p-i-n diode structure, dopant ions, such as boron and phosphorous, are implanted for p and n regions. By using SiO_2 or resist mask, these ions are implanted selectively

and independently into the desired regions. If we would like to construct a Ge photodiode, for example, a vertical Ge p-i-n diode, additional implantation for lower electrodes is also performed at this time. After the implantation masks are removed, the dopants should be activated by high-temperature annealing.

After activation annealing, Ge layers are selectively grown on silicon waveguides or slab regions prepared for Ge active devices. There are several Ge growth methods, such as ultrahigh vacuum chemical vapor deposition (UHV-CVD) [14, 17] and reduced pressure chemical vapor deposition (RP-CVD) [18]. The selective growth is achieved by using a selective growth mask, for which SiO_2 is often used. In order to protect other devices from damage during Ge deposition, complete coverage and endurance against deposition gases are very important issues for selective growth masks. At the final stage of Ge growth, some passivation processes are often added for surface protection and electronic performance improvement. Post-growth annealing is often employed to reduce lattice defects. After the Ge growth, dopants for the electronic contact and for p-n junction are implanted on the top layer of the Ge, followed by an activation annealing. Finally, metallic materials are deposited and etched to make electrode pads both for Si dynamic devices and Ge active devices.

7.3.3 SSCs and Overcladding

After dynamic and active devices are constructed, an overcladding layer is formed with a SiO_2-based material or polymer resin material. To avoid damaging the silicon layer, the cladding layers must be deposited by a low-temperature process, such as the plasma-enhanced chemical vapor deposition (PE-CVD) method [19]. In particular, for waveguides associated with Ge detectors and Si modulators, it is essential to use a low-temperature process so as not to damage their electronic structures. Since a silicon photonic wire waveguide has a very small mode profile, spot-size conversion is essential for connecting the waveguide to external components, such as single-mode optical fibers. As described earlier, highly efficient SSCs with grating couplers [7, 8] or silicon inverse adiabatic tapers [9, 10] have been developed. These SSCs are compatible with the fabrication process described above.

Figure 7.9a shows a scanning electron microscope (SEM) image of the core of a silicon photonic wire waveguide with a cross-section of $400 \times 200\,nm^2$ [10]. The geometrical shape closely matches the design values, and the perpendicularity of the sidewalls is also very good. Figure 7.9b shows a photograph of an 80-nm-wide taper tip in an inverse-taper SSC. The taper may be covered with a silica waveguide core in order to improve coupling efficiency to fibers.

For the silica core for the SSC, an index-controllable silica-based layer must be deposited with the process temperature kept low. Silicon-rich silica (SiO_x) or silicon oxy-nitride (SiON) deposited by the ECR-PECVD method are promising materials for the silica core for the inverse-taper SSC. The ECR plasma dissociates gas molecules efficiently and provides moderate energy to the substrate surface.

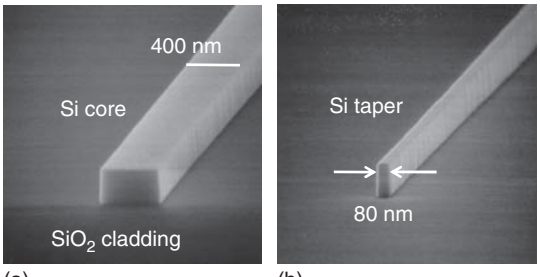

Figure 7.9 SEM images of a silicon photonic wire waveguide system. (a) Core of silicon photonic wire waveguide and (b) silicon taper for SSC.

This enables fast deposition of high-quality and index-controllable silica films at low temperatures. In ECR-PECVD, a mixture of O_2, N_2, and SiH_4 gases is used for the SiON films, and O_2 and SiH_4 gases are used for SiO_x films. The O_2 and N_2 gases are introduced into the plasma chamber and mixed with the SiH_4 gas. In ECR-PECVD, the energy of the ions irradiated to a wafer is about 10–20 eV [19]. This moderate energy induces a reaction on the wafer surface so that high-quality films are formed at low temperatures. As the ECR-PECVD system does not add bias to the substrate, the wafer temperature during the film deposition can be kept below 200 °C even without wafer cooling. To control the refractive index of the deposition films, the flow rate of O_2 and N_2 for SiON films and the flow rate of O_2 for SiO_x films are adjusted with the flow of SiH_4 maintained at a fixed rate. Figure 7.10 shows the refractive index and deposition rate of SiO_x by ECR-PECVD with a SiH_4/O_2 gas mixture. The SiO_x film index can be controlled over a wide range from 1.47 to 1.72 by adjusting only the O_2 flow rate. The deposition rate is about 150 nm min^{-1}, which is high enough for depositing waveguide films. These low-temperature silica-deposition technologies can be used in constructing silica-based waveguides on Si and Ge photonic devices, which cannot endure the conventional high-temperature silica deposition process.

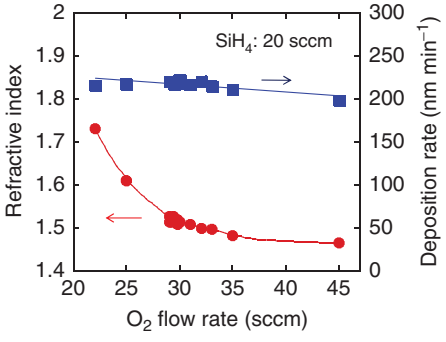

Figure 7.10 Refractive index and deposition rate of SiO_x with changing O_2 and N_2 flow ratio.

7.4
Propagation Performance of Waveguides

Figure 7.11 shows a typical transmission loss of silicon photonic wire waveguides with inverse-taper SSCs [20]. High-NA optical fibers with 4.3-μm MFD are used for external coupling. As shown in this figure, the propagation loss for the TE-like mode has been improved to around 1 dB cm^{-1}. In waveguides with flat cores, the propagation losses for TM-like modes are generally better than those for TE-like modes. The propagation loss of around 1 dB cm^{-1} is already at a practical level, since photonic devices based on silicon photonic wire waveguides are typically smaller than 1 mm. In addition to the sidewall roughness of the core, the core width also affects propagation losses. Figure 7.12 shows the relation between measured propagation loss and core width [21]. As shown, the propagation loss is reduced by increasing the core width, because the effect of sidewall roughness is reduced in a wide core. When the core width exceeds 460 nm, the waveguide can also guide a higher order mode, which may degrade the performance of some photonic devices.

The coupling loss between optical fiber and a silicon photonic wire waveguide is represented by the intercept of the vertical axis in Figure 7.11. The loss value at

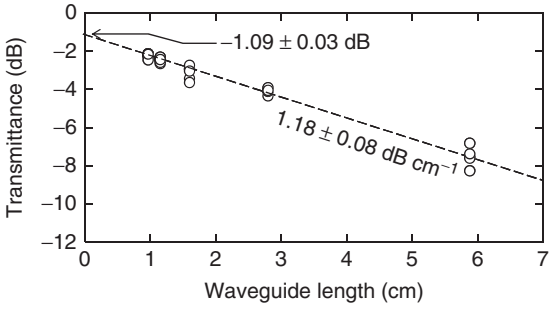

Figure 7.11 Measured transmission loss of a silicon photonic wire waveguide with SSCs.

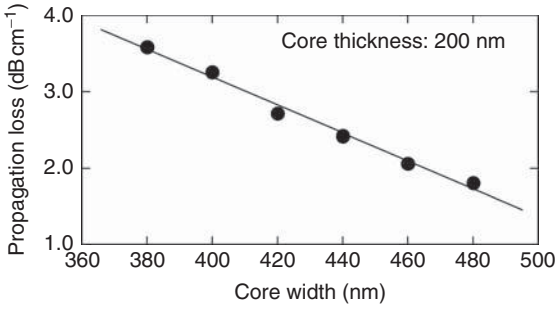

Figure 7.12 Relation between measured propagation loss and core width.

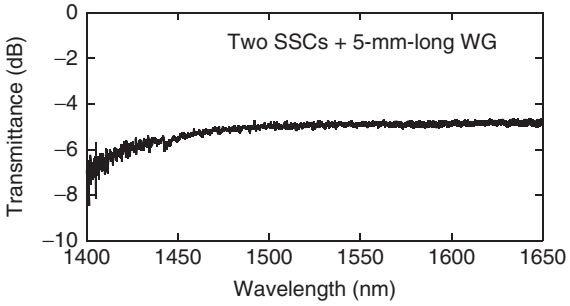

Figure 7.13 Measured transmission spectrum of a typical silicon photonic wire waveguide with SSCs.

the intercept includes two waveguide/fiber interfaces; therefore, in this case, one interface has a 0.5-dB coupling loss at a wavelength of 1550 nm.

Figure 7.13 shows the transmission spectrum of a silicon photonic wire waveguide with two SSCs [1]. The spectrum remains flat over a 200-nm-wide bandwidth, and no absorption dip is observed. The flat spectrum means that the SiO_2-based material used in the SSCs does not contain impurities with N–H bonds. Although absorption by residual O–H bonds exists at wavelengths of around 1400 nm, the resulting losses are not large. It is also possible to eliminate O–H bonds by heat treatment.

Figure 7.14 shows bending losses of single-mode waveguides for TE-like modes [11]. For the bending radius of over 5 μm, bending losses are negligible. Even for an ultrasmall bending radius of around 2 μm, a waveguide with a flat core maintains a low loss of below 0.1 dB per 90° bend. A waveguide with a square core shows a larger bending loss for a bending radius below 5 μm. For TM-like modes, especially in waveguides with flat cores, bending losses are generally larger than

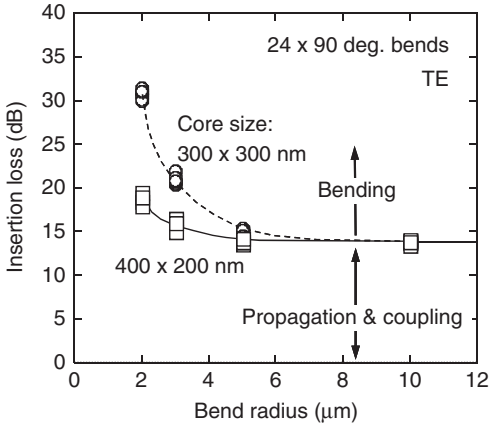

Figure 7.14 Relation between measured insertion losses and bending radius.

those for TE-like modes. Bending losses measured by various research groups are summarized in Ref. [22].

7.5 Integration of Si/Silica and Ge Photonic Devices

7.5.1 Integration of Si-Based Modulation Device and Ge-Based Photodetectors

Integration of modulation devices and photodetectors is very important in practical applications of Si-based photonic systems. For example, optical transceivers require functions for optical data modulation and receiving optical signal. Moreover, optical nodes require functions for monitoring and adjusting optical power. Recently, Si-based modulation devices and Ge-based photodetectors have been monolithically integrated. Figure 7.15 shows an example of monolithic integrations of fast variable optical attenuators (VOAs) and Ge photodiodes [23]. The device consists of a lateral pin Si VOA and a vertical pin Ge photodiode with 3-dB multimode interference tap coupler. Using this device, optical output adjusted by the VOA can be monitored by the on-chip Ge photodiode. Although the 3-dB frequency bandwidth of the VOA is around 100 MHz in this device, a similar Si lateral pin diode structure can also work as a fast optical modulator for a bit rate of over 10 Gbps by applying pre-emphasis electrical input [24].

7.5.2 Integration of Si/Silica-Based Wavelength Filter and Ge-Based Photodetectors

Integration of multichannel optical add/drop filter and photodetectors is very important in constructing optical receivers for wavelength division multiplexing (WDM) telecommunications systems. Recently, AWG-type add/drop filters have been monolithically integrated with Ge photodiode array [25–27]. AWG filters can be constructed by using various waveguiding systems, such as Si, silicon nitride, and silica. In AWG filters based on silicon photonic wire and silicon nitride waveguides, thanks to their strong optical confinement, device size can be reduced significantly; however, it is very difficult to eliminate polarization dependence and polarization diversity systems are needed for achieving polarization-independent performance. In AWG filters based on silica waveguides, thanks to the relaxed

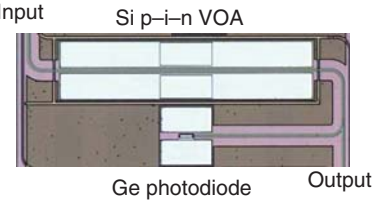

Figure 7.15 Monolithic integration of Si VOA and Ge photodiodes.

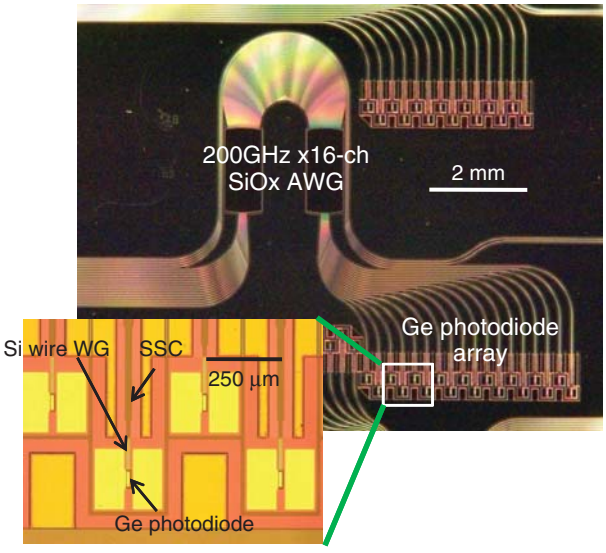

Figure 7.16 Monolithic integration of silica-based AWG and Ge photodiodes.

fabrication tolerance, superior device performance in insertion loss, polarization dependence, wavelength accuracy, and adjacent channel crosstalk are achievable. Therefore, silica-based devices are suitable for telecommunications applications in which very high device performance is required.

Figure 7.16 shows an example of integrations of a silica-based AWG filter and Ge photodiode array [25].

In order to protect Ge devices from thermal damage, silica-based films for the waveguide core and overcladding were deposited by the low-temperature ECR-PECVD method, as described in Section 7.3.3.

7.6 Summary

Si photonic wire waveguides and silica waveguides fabricated by a low-temperature process provide a high-performance, high-density photonics integration platform. On this photonics platform, low-loss photonic wiring, sophisticated passive devices, and dynamic devices with electronic structures have been developed. This photonics platform also has a superior compatibility for constructing Ge-based active photonic devices, and these Si and Ge-based photonic devices can be monolithically integrated on this platform. In the next stage, efforts will mainly shift to a large-scale photonic integration while maintaining the performance of each device. The ultimate goal is, of course, a large-scale electronic-photonic integration, which is the most important advantage of the silicon-based photonic platform.

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8
Detectors

Subal Sahni and Gianlorenzo Masini

8.1
Introduction

Bulk Ge photodetectors have long been considered to be a cheaper, but lower-performance, alternative to InGaAs-based devices for Near InfraRed (NIR) applications. The large progress achieved in monolithic integration of Ge detectors on Si substrates, alongside complementary metal oxide semiconductor (CMOS) electronics in particular, has changed the picture in recent times. Today, several million Ge-on-Si photodetectors are produced yearly and find applications in mission-critical high-performance supercomputer applications. This chapter reviews the state of the art for Ge on Si photodetectors, starting with a historical overview of the key milestones that resulted in today's achievements. A critical comparison of the different processing techniques used to grow Ge films on Si for photodetection applications is then presented, and the different device architectures attempted and demonstrated in the literature with the goal to maximize performance are discussed. Finally, the results of the efforts to monolithically integrate the Ge detectors with the electronics used to process the signals generated by them are also illustrated.

8.2
Historical Background

Early attempts to build a Si/Ge heterojunction diode date back to the 1960s, just about 15 years after the semiconductor revolution had been ignited by the work of the Bell Labs Solid State Physics Group. Oldham *et al.* describe a diode formed by growing a Ge film on Si by Chemical Vapor Deposition (CVD) [1]. The device shows a rectifying characteristic and a bias-dependent photo-response spectrum extending in the infrared down to ~2.5 μm (see Figure 8.1) [2]. The different parts of the spectral response arise from the contribution of the Si substrate, the Ge

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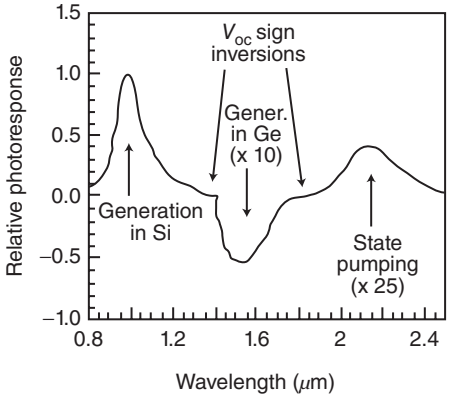


Figure 8.1 Photocurrent spectrum of the first Ge on Si heterojunction photodiode. After [1].

film and, for the longer wavelength part, to the pumping of defect-related gap states. Owing to the doping type used (both Si and Ge are n-type), the device behaves as a couple of backward connected Schottky diodes whose photocurrents move in opposite directions and are quenched/enhanced by opposite bias (see Figure 8.2).

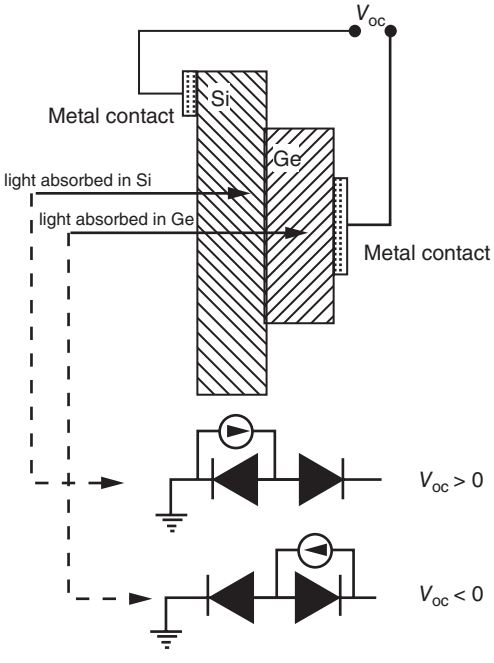


Figure 8.2 Schematic and model of the Ge on Si heterostructure diode evidencing the counterpropagating photoresponses at different bias/wavelength.

8.3
Fiber-Optics Revolution

The interest in Ge on Si heterostructures faded after those initial attempts, only to be revived two decades later, when the beginning of the optical fiber revolution [3] prompted the need for high-performance near-infrared photodiodes working at 1.3 and 1.55 μm. By the early 1980s large progress had been made in epitaxial techniques particularly in the use of buffers to deal with lattice mismatch [4]: Luryi *et al.*, used a thick (1.8 μm) gradual buffer to grow Ge on Si and demonstrated the first p-i-n vertical diode based on this epitaxial film [5]. Quantum efficiency as high as 40% was demonstrated at short circuit and 1300 nm, but with accompanying dark current exceeding 50 mA cm^{-2} at 1 V reverse bias. The latter is about 500 times higher than the value achieved for similar diodes built on bulk Ge wafers, indicating the presence of a relatively high dislocation density in the epitaxial film. In subsequent work, published the next year, the same group attempted the use of a superlattice-based buffer successfully reducing the dislocation and dark current density by two orders of magnitude. However, the photoresponse dropped as well resulting in a mere 3% quantum efficiency [6].

With the focus of optical communications on the 1.3 μm window, and the promising results showing the possibility of exceeding the critical thickness by growing strained superlattices (SLSs, [7]), a number of groups attempted the fabrication of NIR photodiodes based on SiGe rather than pure Ge. In some cases a waveguide configuration was used to compensate for the lower absorption coefficient. In [8, 9] devices using different amounts of Ge in a SLS structure were reported with a maximum external quantum efficiency exceeding 10% at 1.3 μm but with the need for a relatively high reverse bias of 10 V, pointing toward issues transporting carriers across the SLS. The best photoresponse was obtained for a 60% SiGe alloy, and as expected, the photoresponse decreased with decreasing Ge content in the SiGe layers. The devices showed a reasonably low dark current of 7 mA cm^{-2} and a ~300 ps pulse response.

8.4
Avalanche Devices

In the same years, prompted by the successful demonstration of III–V Separate Absorption and Multiplication (SAM) Avalanche PhotoDiodes (APDs) [10], the first attempt to combine the excellent avalanche properties of Si (very high ratio between ionization coefficient of electrons and holes, [11]) with the strong absorption efficiency in the NIR of Ge was published [12, 13]. The device used a SiGe SLS absorption region to reduce dark current and demonstrated a maximum responsivity of 1.1 A W^{-1} at 1.3 μm with a reverse bias of 30 V. A slightly optimized device with an inverted doping stack improved on that value by reaching 4 A W^{-1} and a response speed of 100 ps [14]. The device was utilized in a test optical link working

at 800 Mb s^{-1} where it reached a sensitivity of −29.8 dBm, close to that of III–V-based PIN receivers [15]. It is interesting to note that, in an attempt to further improve the responsivity of the SLS-based device, the authors employed it in forward bias where a strong photoresistive gain was observed, probably due to the dispersive transport of holes through the SLS. Despite the large gain, the high dark current associated with forward bias diffusion resulted in a degraded sensitivity for the receiver [16].

An in-depth study of ionization coefficients for electrons and holes in SiGe alloys (up to 100% Ge) can be found in [17] in which SiGe p-i-n and n-i-p devices were grown on Si substrates by Molecular Beam Epitaxy (MBE). The Authors found a ratio between the ionization coefficient of electrons (α_n) and holes (α_p) ranging from 10 (for pure Si) to 0.75 (for pure Ge).

Short period Si–Ge superlattices were attempted as a way to increase absorption (by the zone folding mechanism [18, 19]) while maintaining high crystal quality and, therefore, low dark current [20]. However, the measured photoresponse did not show the expected enhancement in the NIR.

8.5 Si-Photonics

The 1990s witnessed a renewed effort in the field of Ge on Si photodetection with European groups joining forces with American ones. The discovery of light emission from porous silicon in these years [21] triggered a large amount of enthusiasm (and flow of money) in the then just-born Si-photonics community, and a number of papers were published.

In Germany, Splett *et al.*, fabricated a waveguide photodetector where guiding was obtained by alloying a small amount of Ge (2%) to Si, while the absorption region comprised a 20-period, $Si_{65}Ge_{45}$ MQW, each 5 nm thick. The device showed a maximum of 11% external quantum efficiency at 1.3 μm and 7 V reverse bias, while the dark current was 1 mA cm^{-2} [22]. A similar device was demonstrated in the same year by a joint collaboration between UCLA and AT&T [23]. In this case also the voltage required to attain reasonable photoresponse was quite high (14 V) possibly due to trapping of holes in the valence band wells created at the Si/SiGe interfaces. Another SiGe superlattice-based device was published in the same timeframe in [24], with similar performance and characteristics. In 1994, the group of von Känel in Switzerland published a paper in which a pure Ge detector was fabricated on a Si substrate using a thin, (50 nm) abrupt, low temperature (420 °C) buffer in an MBE system [25]. The device performed similarly to the one originally demonstrated by the Bell Labs group [5], despite the simpler fabrication process used, with good responsivity extending down to 1.6 μm and a dark current of 50 mA cm^{-2}.

In the same years, possibly motivated by the success of using a small amount of carbon in the SiGe alloys forming the base layer of Heterojunction Bipolar Transistors (HBTs), a few groups attempted the use of SiGeC alloys for photodetection.

The rationale supporting the use of carbon is the possibility to tune the alloy lattice parameter thus reducing the mismatch with the Si substrate [26]. Unfortunately, carbon solubility in SiGe is pretty low, and alloying results in the widening of the bandgap thus defying the effort to extend the photoresponse toward longer wavelengths. To overcome the first issue, a non-equilibrium growth technique must be used, such as MBE (or CVD at very low substrate temperature). The device reported in [27] used 1.5% carbon in a SiGe alloy with 60% Ge; however, both electrical and optical characteristics were not very different from those of similar devices using only SiGe materials. In particular, the reported quantum efficiency at 1.3 μm was only 1%, at normal incidence.

A similar attempt, using the results of an optimization study published in [28] and considering alloy composition within the critical thickness constraint, is reported in [29]. GeC alloy (no Si) was used in [30] to build a heterostructure photodetector. Thanks to the large amount of Ge in the film the photoresponse extended to 1.5 μm with a peak responsivity of 35 mA W^{-1} at 1.3 μm. Despite the high dislocation density (10^{10} cm^{-2}) observed by TEM, the dark current was limited to few mA cm^{-2} at 1 V reverse bias.

The first report of a SiGe detector grown on an SOI substrate and using a waveguide configuration appeared in 1997 [31]. The device used a low-Ge content (10%) SiGe SLS and exhibited a 25% quantum efficiency at 980 nm with low dark current of 50 μA cm^{-2}. Owing to the low Ge content the photoresponse did not extend to the second and third windows.

8.6 High-Performance Ge Detectors

By the end of the 1990s the focus of research groups was directed once again toward devices based on pure Ge and, therefore, capable of operating in the third window of optical communication. In 1998, devices with very low dislocation density were reported using a combination of long, gradual buffers and Chemical-Mechanical Polishing (CMP) on miscut Si wafers [32]. The vertical PIN device based on that material exhibited record-low dark current better than 0.2 mA cm^{-2} and reasonable responsivity, given the non-optimal thickness of the film. In the same year, the two-step growth method, which quickly became the standard for Ge-on-Si CVD epitaxy was introduced [33, 34]. The technique consists of a first step where a thin, pure Ge, film is grown at 350 – 400 °C directly on the Si substrate. Thanks to the low mobility of precursors on the Si surface at this temperature, 3D growth is inhibited and a flat film is obtained. The film thickness is chosen such that a full relaxation is obtained, mostly through the introduction of misfit dislocations at the Si/Ge interface. In the second step the temperature is raised to above 550 °C thus allowing fast growth of high-quality material on the relaxed buffer. Material quality can be further improved by using cyclic thermal annealing [35], with consequent improvement of device performance [36].

The promising results obtained by these techniques opened the way to the industrialization of the growth process and, with time, to the debut of the first commercial Ge on Si photodetector toward the end of the first decade of the twenty-first century.

8.7 Process Options and Challenges

Ge films can be grown on Si using different techniques: in addition to the classic CVD and MBE, along with all the associated variations, new techniques such as Ge condensation and Rapid Melt Growth (RMG) have been recently introduced. This section summarizes the results obtained using different processing approaches and the challenges associated with each one.

8.7.1 Physical Vapor Deposition (PVD)

The PVD definition includes a number of rather different techniques spanning from the highly sophisticated MBE, capable of layer-by-layer control and epitaxial growth to sputtering, normally used to grow amorphous or polycrystalline films. Thermal evaporation is, probably, the simplest form of PVD. Ge films grown by evaporation show polycrystalline quality as soon as the substrate temperature exceeds 250 °C, as demonstrated by the Raman spectra [37]. Because of large defectivity, these films have relatively high p-type conductivity (the Fermi level is pinned closed to the valence band by defect states), and quite short diffusion length. As a result, Ge/Si photodetectors built using this approach suffer from low quantum efficiency [38]. The latter can be enhanced by using a waveguide configuration [39], but even in the best devices, the performance is still far from that attainable with high quality, mono-crystalline materials. In a recent report, a large increase in responsivity was observed by compensating the p-type conductivity using n-type doping [40]. The doping was achieved by the diffusion of phosphorous from a spin-on film source at relatively low temperature (580 °C). A 0.1 A W^{-1} responsivity at 1.55 μm is quoted, albeit with a relatively large dark current, potentially due to the weakly blocking nGe/nSi heterojunction configuration of the fabricated device.

As mentioned in the historical background chapter, MBE has been widely used to build complex, multi-layer, film structures spanning from Multi-Quantum Wells (MQWs) to superlattices, all aimed at improving the absorption characteristics of the material in the NIR while maintaining structural integrity and reducing dislocation count. The technique is particularly powerful in controlling the layer growth down to the single atomic thickness (see, for example, a high-resolution XTEM of a SiGe superlattice in Figure 8.3 [41]); however, it has never gained large popularity in the Si industry and its use is mostly limited to research labs. The need for ultra-high vacuum (UHV) conditions and the intrinsic

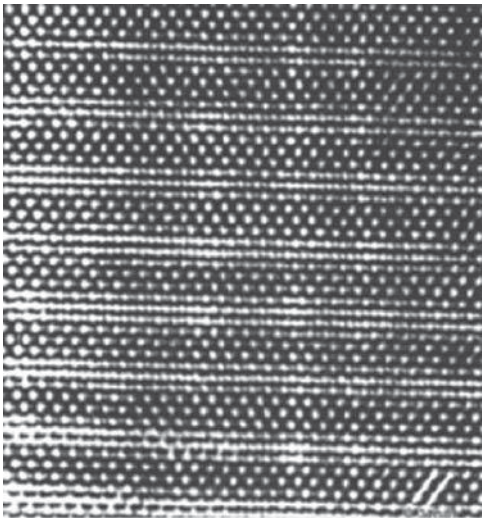


Figure 8.3 XTEM of a Si_5Ge_5 superlattice. Reproduced from [41].

small-area, single-wafer, operation mode are among the reasons for the lack of adoption by the Si foundries. The growth of SiGe films on Si substrates can be helped in MBE systems by the use of a group V element (As, Bi, Sb) as a surfactant [42] that, by reducing the surface energy, helps avoid the aggregation of ad-atoms and the resulting 3D growth. The disadvantage of this technique remains in the incorporation of the surfactant atoms in the growing film resulting in a residual n-type doping [43].

In recent years, a record high-speed Ge on Si photodetectors has been demonstrated based on material grown in MBE systems: in [44] an RC-limited bandwidth of 38.9 GHz is reported, while a few years later, the same group achieved 49 GHz for a device with active area diameter of 10 μm [45]. Both devices use a p-i-n vertical configuration and are grown on a p-type Si substrate. A relatively thin (300 nm) p+ doped layer is used both as a buffer layer (to absorb the lattice mismatch through the introduction of misfit dislocations) and as the anode of the device. This arrangement confines the defective material into the highly doped anode that never gets depleted under normal operation thus reducing the detrimental effect of defects on dark current (generation) and speed (mobility). To avoid transit-time limitations, the active (intrinsic) region of these diodes is kept to 330 nm which, being much shorter than the absorption length at the tested wavelength of 1.5 μm, results in a penalized responsivity of 50 mA W^{-1}. This limitation can be overcome by using a waveguide configuration as discussed below.

Finally, the sputtering technique (DC-pulsed magnetron, in this case) has also been used to produce epitaxial Ge films on Si and demonstrate photodetectors in [46]. The results indicate that relatively high film quality can be obtained with this technique which, in its many incarnations, enjoys a quite broad acceptance in the semiconductor industry.

8.7.2 Chemical Vapor Deposition

CVD is by far the most common technique used for epitaxial film growth, particularly in an industrial environment. Though initially research groups mostly relied on UHV CVD systems to grow SiGe films on Si, today the use of single-wafer, reduced- or atmospheric-pressure systems is widespread. In fact, despite its better control on impurity and layer growth, UHV-CVD has the disadvantage of requiring a more sophisticated vacuum system and of slower temperature control. CVD systems are commonly found in Si foundries nowadays and are mostly used to deposit the stressor films used in the source/drain regions of modern PMOS transistors and/or to grow the SiGe base in HBTs used in BiCMOS technologies. This fact makes CVD the process of choice for the integration of Ge detectors in a standard CMOS flow.

Typical gas precursors used in the CVD growth of SiGe films are silane (SiH_4) and germane (GeH_4), though higher order compounds are sometimes used, especially to replace silane, when lower substrate temperature and high deposition rates are desired [47]. At low substrate temperature, the hydrogen derived from the reaction of the gas precursor tends to act as a surfactant thus suppressing island formation [48]. Recently, the use of Phosphorous (through decomposition of phosphine, PH_3) has also been reported to have surfactant effects. Similar to MBE, part of the surfactant is alloyed in the growing film resulting in n-type doping [49].

One of the advantages of CVD over PVD techniques is the possibility to obtain large nucleation selectivity between Si and dielectric surfaces thus allowing localized growth of films on patterned substrates. This is particularly useful when devices such as germanium photodetectors have to be integrated with other components on the same wafer. Selectivity in CVD can be naturally obtained because of the mild etching effect of the atomic hydrogen, generated during the precursor reaction, which removes the poly-crystalline phase that nucleates on the dielectric surfaces. This is particularly true at low chamber pressure, below 100 Torr. Better results can be achieved by using chlorinated precursors and/or adding HCl to the gas mixture [50]. In addition, selectivity is typically observed to be more pronounced to silicon oxide, rather than to nitride [51], which can be a challenge as the choice of the dielectric stack used to create selective epitaxial regions for Ge in a typical CMOS process is limited to that dictated by the use of oxide (fillers) and nitride (etch stop, spacers) films for the other integrated components. When selective epitaxy is used, the density of open windows may affect the growth speed locally and globally, thus resulting in non-uniform film thickness across the wafer and the need to retarget the growth conditions for different mask sets [52]. These issues can be alleviated by either using dummy filler windows uniformly distributed across the wafer (where possible, avoiding interaction with other components), or by working in the zero-area approximation with few, widely spaced windows. The latter is generally achieved in integrated transceivers where just a small number of detectors are integrated on the CMOS IC. The waveguide photodetector reported in [51] is

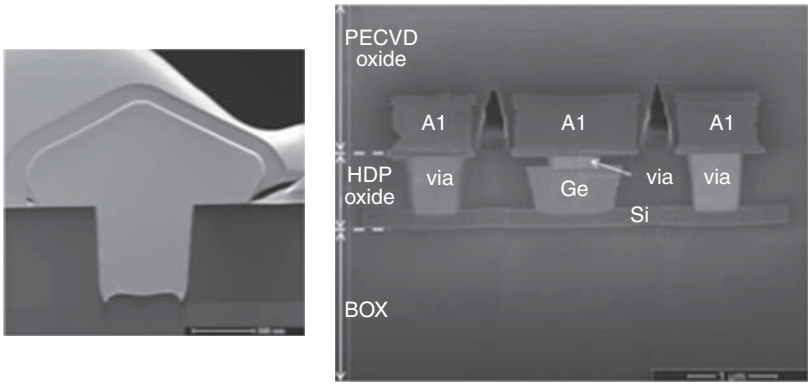


Figure 8.4 Cross-section of the Ge film used in [53] as deposited using a selective process (a) and after CMP and device fabrication (b).

based on epitaxial Ge selectively grown by CVD using a patterned oxide layer as the growth mask. Because of the above-mentioned issues with controlling the growth rate on a patterned substrate, the authors used a process in which the Ge film is overgrown above the edge of the dielectric window and is, then planarized using a CMP step. The film is grown using the two-step technique [33] to avoid 3D growth, and, in order to reduce the dislocation density an annealing step at 750 °C for 1 h in H_2 atmosphere is used [35]. A similar approach was used in the waveguide photodiode described in [53]. Figure 8.4 shows the overgrown Ge film before (a) and after (b) the CMP process.

A key step in successful epitaxial growth is the cleaning and preparation of the substrate. The presence of contaminants as well as roughness and topography heavily affect the quality (defectivity) and morphology of the growing film. The subject of pre-epi surface cleaning is very wide and we will just mention some key facts here pertaining to the growth of Ge films on Si substrates. Typical "contaminants" observed on a Si wafer that interacts with the epitaxial growth of Ge are Oxygen and Carbon. The first is typically captured from atmospheric O_2 and H_2O molecules by bare Si surfaces forming native oxide [54], while the second is frequently found as a by-product of Si processing (plasma etch) using polymeric masking films (photoresist). While the presence of nanoscopic SiO_2 "platelets" has been used in the past to help the growth of non-commensurate materials (such as Ge on Si) [55], it is usually found that concentration of O and C at the substrate surface must be kept below 10^{19} cm^{-3}. This is normally achieved through a two-step cleaning process: the Si substrate is first cleaned in a wet bench with the goal of removing a small amount of the exposed material thus exposing a bare surface, and then once the wafer is loaded in the epi tool, a second, *in-situ* clean is performed. The first step can be accomplished by a classic RCA clean [56] followed by an HF bath to produce an oxide-free, H-terminated Si surface. Depending on the process used, this surface can be stable in air for several hours,

which is a requirement for ensuring manufacturability. The second cleaning step is typically performed by baking *in-situ* the substrate at $T > 800\,^{\circ}C$ in an H_2 atmosphere (H_2-bake). Because of the process integration issues related to the use of the high-temperature H_2-bake, alternative techniques based on the reaction of Ge with contaminants followed by the removal of the formed compounds by a flow of HCl have been proposed [57, 58]. These techniques have been shown to produce an epi-ready surface at much lower substrate temperature (<700 °C) and are, therefore, very attractive for integration.

Standard CVD relies on substrate temperature to provide the energy required to break the gas precursor bonds and initiate the reaction with the surface. By adding another source of energy, independent of temperature, some of the tradeoffs such as the one existing between growth rate and film quality, for instance, can be relaxed. The most common method of supplying energy to break the precursor molecular bonds is through the action of plasma. In typical Plasma Enhanced CVD a glow discharge is generated in the gas mixture by the action of an external RF source (usually oscillating at 13.56 MHz). SiGe and Ge films can be deposited using this technique at very low substrate temperatures (<250 °C), though they are normally amorphous or polycrystalline and contain a high percentage of hydrogen. The latter widely modifies the band structure shifting the absorption edge to shorter wavelengths (~1 eV for a-Ge:H [59]). As a consequence, hydrogenated-amorphous Ge films are not suitable for efficient absorption in the second and third windows of the optical communication. However, if the plasma energy is kept to a minimum and it is balanced with higher substrate temperature, high-quality crystalline films can be grown: the technique, introduced in [60] is named Low-Energy Plasma-Enhanced Chemical Vapor Deposition (LEPECVD). The Ge on Si photodiodes fabricated using this technique exhibit record low dark current of 40 μA cm^{-2} at 1 V reverse bias with a responsivity of 0.4 A W^{-1} at 1.55 μm [61]. The devices have a vertical p-i-n structure with a 1 μm thick intrinsic layer and were subjected to three cycles of thermal annealing between the temperatures of 600 and 780 °C to reduce the dislocation density. A large improvement of two orders of magnitude in dark current was observed for the annealed devices. The beneficial effect of post-growth anneal on Ge on Si diodes is discussed in details in [62]. Figure 8.5 show the IV characteristics of diodes subjected to annealing steps at different temperature.

Owing to the difference in the thermal expansion coefficients of Si and Ge, films of the latter deposited at relatively high temperature on Si substrates experience a tensile stress when brought back to room temperature. The strain induces a modification in the band structure resulting in a narrower bandgap. This effect helps extending the photoresponse toward longer wavelengths [63].

8.7.3 Rapid Melt Growth

One of the obstacles in integrating the growth of Ge films into a standard, poly-gate CMOS process is the presence of a high temperature anneal used after gate

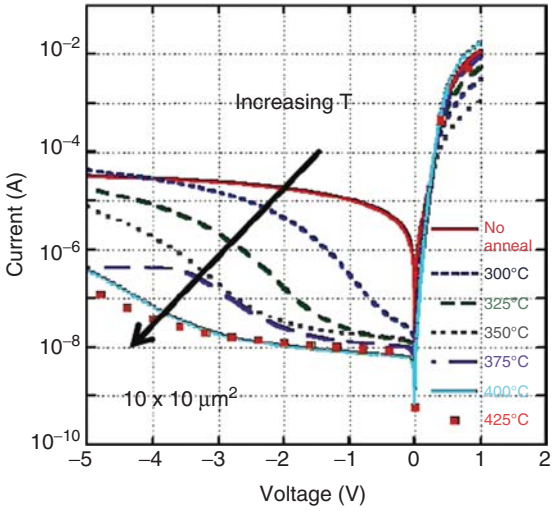


Figure 8.5 Effect of thermal anneal on the dark current of a Ge on Si diode [62]. Reproduced with permission from [62]. Copyright [2012], AIP Publishing LLC.

formation to improve the quality of the poly-Si film. This step is normally performed at a temperature of ~1000 °C, which can be detrimental for an existing epitaxial Ge film. This is the reason why the Ge epitaxy is normally delayed until after gate formation. However, under appropriate conditions, the same anneal has been shown to produce high-quality crystalline films by RMG. In this technique, an amorphous Ge film is deposited on a Si wafer covered by a patterned dielectric. The film is then capped and subjected to a spike anneal during which the Ge melts and solidifies starting at the regions in contact with the substrate. The lower thermal resistance in these windows generates a crystallization front propagating to the rest of the film standing on the dielectric: relaxation of lattice mismatch occurs in the first few nanometers of the growth thus leaving the rest of film free of dislocations [64]. RMG has been used to demonstrate high-performance waveguide photodetectors using a Metal-Semiconductor-Metal (MSM) configuration in [65]. A cross section of the Ge film resulting from RMG is shown in Figure 8.6.

8.7.4 Other Techniques

A completely different approach to obtaining epitaxial Ge films on Si substrates is a process known as Ge condensation [66], which uses the preferential oxidation of Si in a SiGe film, resulting in the segregation of Ge atoms and eventual production of a pure Ge film. A Ge photodiode based on this process is demonstrated in [67]. The device has an MSM structure and shows very low dark current; however, the photoresponse, extending to 1550 nm, is also quite low, mostly because of the thickness of the film (12 nm) being much smaller than the absorption length.

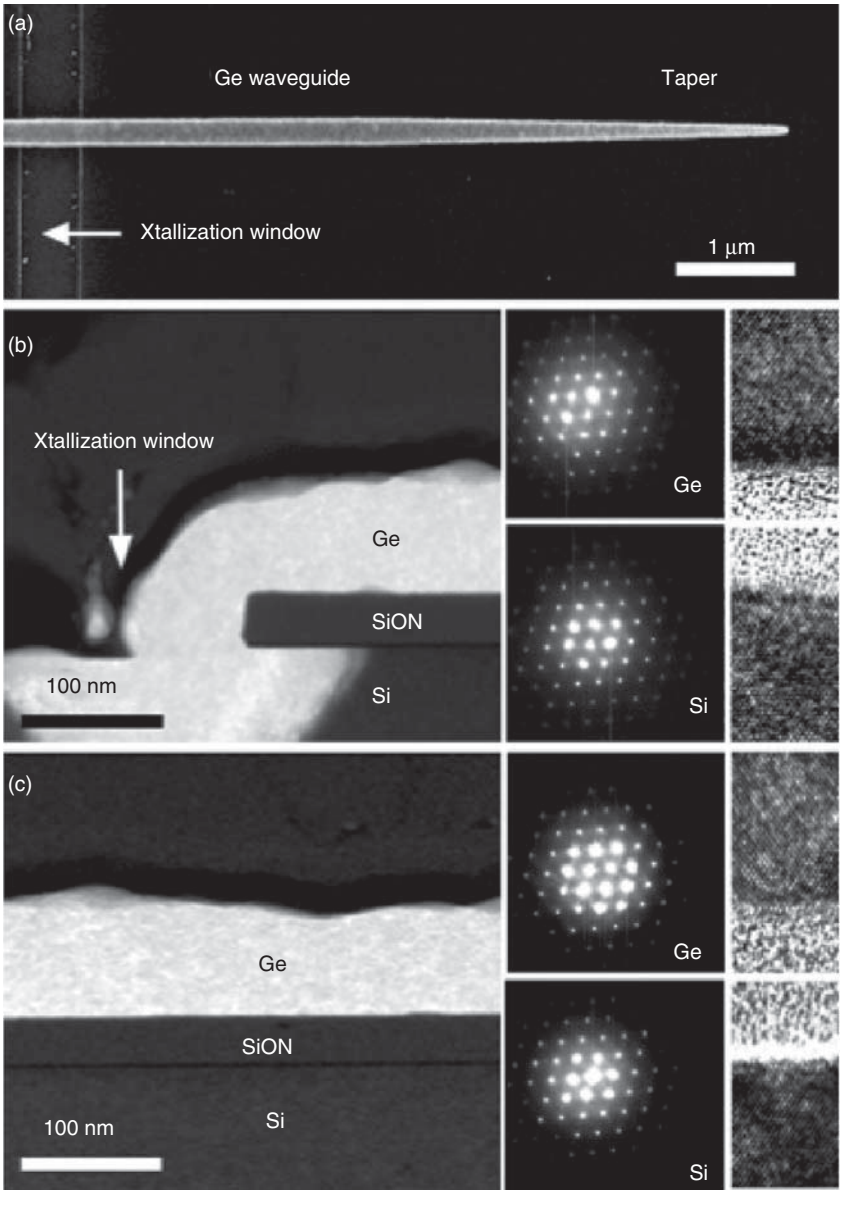
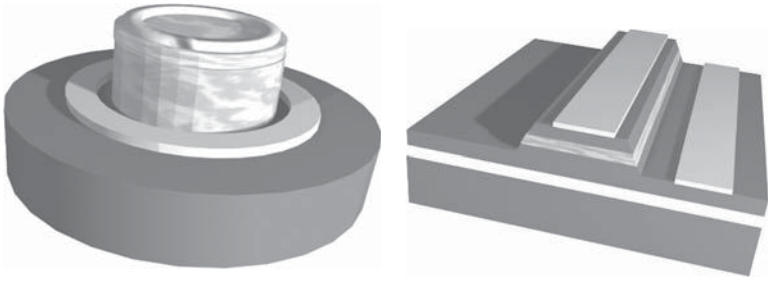


Figure 8.6 Ge waveguide on Si fabricated using the rapid melt growth technique [64] top view (a), side view close to the seed window (b), side view along the waveguide (c).

Finally, crystalline Ge films can be placed on a Si substrate using a layer transfer technique similar to the SmartCut® process used to fabricate SOI wafers [68]. In this approach, a Ge wafer is heavily implanted with hydrogen to create a preferential delamination plane at a certain distance from the surface. The wafer is then flipped and bonded to a Si wafer, a fracturing plane is created in correspondence of the peak of the implanted hydrogen by a thermal process and the thick substrate is removed. The exposed surface can then be polished and thinned down to the desired thickness. The process is sometimes referred to as exfoliation [69]. The vertical heterojunction diode described in [70] is based on a Ge on Si film produced by the exfoliation technique. The junction is formed between the n-type Si substrate and the p-type Ge film and exhibits good rectifying characteristics with a dark current of ~100 mA cm^{-2} at 1 V reverse bias. No optical characterization was reported.

8.8
Device Architectures

Photodetectors can be broadly classified into "surface illuminated" and "waveguide" (see Figure 8.7) based on the method used to couple light into the absorption region Surface illuminated detectors are normally used in focal plane arrays (imaging) and as discrete components for optical communications up to ~25 Gbps. In waveguide photodetectors, the light is confined to the directions perpendicular to propagation thus allowing for a more compact design and smaller junction area. Of course, unless the light is already traveling in a waveguide integrated on the same substrate as the detector, the waveguide photodetector requires much tighter alignment tolerances for the incident light beam. Typical surface illuminated photodetectors use a vertical p–i–n architecture in which light and current travel in the same direction. This configuration forces a trade-off between speed (transit time) and responsivity (through the absorption length) that can be avoided by using the waveguide configuration in which the photocurrent travels perpendicularly to the propagating light (see Figure 8.8). In addition, surface illuminated



(a) (b)

Figure 8.7 Surface illuminated (a) and waveguide (b) optical configurations.

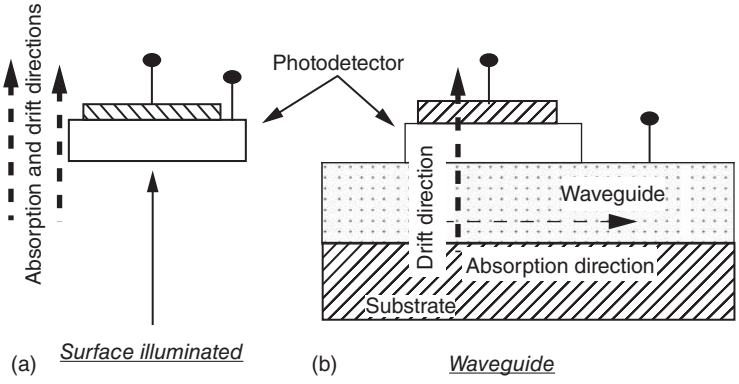


Figure 8.8 In a surface-illuminated detector (a) the absorption and drift directions are parallel resulting in a trade-off between responsivity and speed. This trade off is relaxed in the waveguide configuration (b).

detectors tend to suffer from larger capacitance because of the requirements on junction area dictated by the size of the optical beam coming out of an optical fiber, which, even in the case of single-mode fibers, is much wider than a typical waveguide mode size. Photodetector capacitance plays a key role in setting the bandwidth/sensitivity trade-off of high data-rate Transimpedance Amplifier receivers [71]: the lower the capacitance, the larger the transimpedance gain can grow without impacting the bandwidth. The higher gain helps improve the S/N ratio thus increasing sensitivity. The waveguide configuration is therefore strongly preferred in the integrated optics systems where the light is already traveling in a waveguide thus simplifying the coupling. Additionally, there has also been some strong progress in making Ge–Si detectors on large core Si waveguides, in order to alleviate the external coupling issue [72].

Several different electrical configurations can be used to fabricate a Ge on Si photodetector: beyond the pn or p–i–n junction diodes, a number of more complex devices have been attempted, in most cases with the goal of increasing sensitivity by means of some form of gain. APDs and phototransistors belong to this class of devices and will be discussed later in this section. Sometimes, aiming at simplifying the device fabrication process, MSM diodes have been used as well. MSM devices are frequently used with wide bandgap semiconductors because of the large obtainable Schottky barrier that results in relatively low leakage [73]. When fabricated on lower bandgap semiconductors, such as Ge, the leakage is normally very high, especially because of the tendency of Ge to pin the Fermi level close to the valence band at the surface [74, 75]. One of the most interesting features of MSM devices is the possibility to achieve very fast response thanks to the short transit time (provided the electrodes are closely spaced). The MSM detector described in [64] is a good example of the characteristics discussed above: it shows a wide bandwidth of 35 GHz (with an open eye at 40 Gbps) but has quite large dark current that is highly dependent on the applied bias as is typical for weakly rectifying junctions. The author's analysis of the temperature dependence of the dark

current confirms that the Schottky barrier at the metal–semiconductor interface is just less than 150 meV. A study on dark current reduction by electrode geometry optimization in Ge on Si MSM photodetectors can be found in [76].

A particular case of an MSM photodetector is described in [77] where a Ge nano-wire is contacted by two miniaturized electrodes shaped so as to act as a dipole antenna working at the frequency of light in the NIR. The authors demonstrate an enhancement factor of 20 for the device responsivity thanks to the antenna effect.

Leakage can be greatly reduced if blocking junctions are formed by doping the Ge film. Being a group IV semiconductor, Ge (and SiGe) share doping species with Si. In particular, Boron acts as a p-type dopant, and can be introduced both by ion implantation [78] as well as *insitu* during the epitaxial growth [79]. Activation is very high even at high doses and low annealing temperatures. When it comes to n-type doping, P is preferred to Sb and As although reaching high activated concentration levels and limiting very fast concentration-dependent diffusion pose significant challenges in Ge when compared to Si [80]. Typical Ge on Si photodiodes have a vertical [45] or horizontal [81] p–i–n electrical structure where the intrinsic (undoped) layer is depleted by the built-in field generated by the opposite doped contacts and provides the optical absorption region. The width or thickness of the intrinsic layer, that is, the spacing between the n-type and p-type doped contacts, determines the trade-off between capacitance and transit time, where both affect the speed of the device [82].

The simple homo-junction p–i–n structure can be extended in a Ge on Si photodetector if one (or both) the electrodes are formed on the Si substrate thus forcing the carriers to travel across the heterojunction. This approach has been used in [83] to demonstrate high-performance photodiodes using highly doped Si substrates. A study of the optoelectronic characteristics of Ge–Si heterojunction photodiodes, as a function of the type and level of the Si substrate doping can be found in [84]. The authors observed a larger sensitivity of dark current and photoresponse on the level of Si doping for n-type substrates, or equivalently, on the density of interface states at the heterojunction. Devices grown both on highly doped p-type and n-type substrates exhibited high responsivity. More recent reports indicate a clear difference between n-type and p-type Si [61] likely due to the large barrier for the injection of photogenerated holes into the Si substrate due to the valence band discontinuity [85] penalizing the p-type substrate configuration. The discrepancy is probably due to a lower level of defectivity at the Si/Ge interface in the latter case resulting in a closer-to-ideal heterojunction behavior.

Si/Ge heterojunctions have also been proposed for SAM APDs in which the superior quality of Si as an avalanche semiconductor [11] is complemented by the high absorption efficiency of Ge in the NIR. As the ionization coefficient of electrons is much higher than that of holes in Si, the best results in terms of sensitivity are obtained when the multiplication process is initiated by a photogenerated electron which, in a Ge/Si SAM-APD corresponds to a configuration with the anode in the Ge film and the cathode in the Si substrate. SAM-APDs with performance exceeding those of similar III–V based devices are described in [86]

(surface illuminated) and [87] (waveguide). Though the above devices are optimized for use in long-haul optical communication links, similar SAM-APDs have also been proposed as single-photon detectors working in Geiger-mode in [88]. In this operating regime, the device is carefully biased above the breakdown voltage where it remains until either an absorbed photon or a thermal event generates an electron-hole pair that initiates the avalanche process and generates a large current pulse [89]. A typical figure of merit for Geiger-mode APDs is the Dark Count Rate (DCR), which sets the maximum length of the observation time window after which an avalanche generated by the dark current itself is very likely to occur and require that the bias across the detector be reset. The Ge on Si APD described in [87] shows a DCR of ~300 kHz at a temperature of 200 K which is only slightly worse than that measured on III – V based devices.

Another device architecture that can utilize the band alignment of the Si/Ge hetero-structure is a photo-transistor. Sahni *et al.* [90] shows the results for a photo-JFET, where the gate in a conventional Si JFET is replaced by an un-contacted island of Germanium. The valence band discontinuity at the hetero-interface results in charge trapping, which can provide significant photocurrent gain, and the transistor architecture enables high bandwidth with suitable channel scaling. The devices reported show significant DC gain (the demonstrated responsivity is ~5 A W^{-1}) and rise times of ~40 ps for 1 μm long channels, but suffer from extremely small absorption cross-sections and poor fall times owing to long-lived trapping (several 10 s of ns). A similar device architecture was also proposed and demonstrated in Ref. [91], where instead of a Si/Ge interface, a MOSFET was constructed with a poly-Ge film acting as the photo-sensitive gate. The DC photocurrent gain, which in this case is the ratio of channel to gate current in the presence of light, was demonstrated to be ~1000. The simulated impulse response FWHM for a 100 nm long channel was shown to be ~100 ps.

8.9 Ge on Si Detectors in Highly Integrated Systems

One of the most interesting aspects of monolithic integration is the ability to fabricate a large number of nominally identical devices in a small area. This can be quite useful in large channel count WDM receivers as well as in systems using complex modulation techniques such as Dual Polarization Dual Quadrature. Ge on Si waveguide photodetectors are used in the 8-channel Coarse WDM system described in [92] and in a 40-channel Dense WDM circuit reported in [93]. The devices are grown using a selective CVD process and have a vertical p – i – n configuration with the cathode in the relatively thick (850 nm) Ge film and the anode in the Si substrate. They show low dark current (~600 nA) at 1 V reverse bias and high responsivity but relatively low speed (~5 GHz bandwidth) possibly limited by the transit time in the thick Ge film [94]. Recently, the possibility of using multi-core fibers (MCFs) [95] has spurred large interest in integrated optical receivers that can handle in a compact space the large data traffic transported by

these fibers. A 7-channel, polarization insensitive MCF receiver using Ge photodetectors is reported in [96]. The system uses polarization splitting grating couplers to deal with the random incoming polarization of single mode fibers: these couplers route the two orthogonal polarizations into two different waveguides that are, in turn, connected to the two inputs of a waveguide Ge photodetector. An MZI-based demux is also integrated in each channel to enable coarse WDM operation (two-channels at 1490 and 1510 nm) and error free operation at 5 Gb s^{-1} per fiber/wavelength (total 70 Gbs) is demonstrated.

Integration of electronics and Ge detectors on the same substrate has several system-level advantages, the most important being the dramatic reduction of parasitics (capacitance, inductance), which enables reaching sensitivity levels unattainable in discrete/hybrid solutions. Si-based detectors for operation at 850 nm showing a high level of monolithic integration have been demonstrated. Nemecek *et al.* [97] show results for surface-illuminated Si detectors integrated into a slightly modified BiCMOS process and interfaced with a monolithic receiver. Integration of pure Ge films is more complex, especially because of the tight thermal budget constraints present in a standard CMOS process, and the relatively low melting point of Ge. An example of monolithic integration of Ge, and the related challenges, is reported in [98] in which waveguide Ge photodetectors are integrated in a 130 nm CMOS process using SOI substrates. Ge is grown using the RMG approach described earlier in this chapter.

One of the more successful commercial implementations of monolithic Ge-on-Si detectors so far has been in Active Optical Cable (AOC) assemblies shipped by Luxtera (and subsequently by Molex Inc, employing Luxtera chipsets, see Figure 8.9) that provide four duplex transmit-receive lanes over eight single-mode fibers, over distances up to a few kilometers [99]. The fibers are connected to electrical interfaces at each end through CMOS photonic transceiver chips that perform the high speed OE–EO conversion. The modules housing the transceivers are compliant with the Quad Small Form-factor Pluggable MSA

Figure 8.9 An active optical cable based on Luxtera chipset integrating Ge photodetectors for high-speed and monitor purposes.

standard, which is used extensively in Infiniband-based high-performance computing applications. The first two generations of transceiver chips manufactured by Luxtera have been used in 4×10 Gbps and 4×14 Gbps AOCs, with [100] reporting on the experimental demonstration of a 4×25 Gbps module. The transceivers employ Si/Ge photo-detectors in multiple roles (details regarding Luxtera's approach to the integration of 100% Ge in a standard CMOS process are in [101]). In each transmit-receive channel, homo-junction PIN Ge-on-Si waveguide photo-detectors are utilized as high-speed photo-diodes in the receiver sub-system and as monitor photo-diodes in the transmitter block, where they are used to provide feedback to both the laser-power and Mach–Zender modulator quadrature control loops. The detectors have responsivity $>0.8\ \mathrm{A\,W^{-1}}$ and dark current $<10\ \mu$A @1 V reverse bias, and provide an electrical bandwidth of about 20 GHz. The Rx analog design benefits greatly [70] from the low capacitance of the monolithically integrated detectors (<10 fF), and the resulting receivers have electrical sensitivity of ~ -24 dBm at 10 Gbps and -21 dB at 14 Gbps (10^{-12} BER). Transceivers with several Ge detectors on each chip have been widely deployed, with Luxtera reporting 10 Gbps lane shipments exceeding a million units in early 2012 [102].

Beyond optical communications, focal plane arrays also take advantage of the integration level offered by monolithic Ge on Si. NIR imagers are usually fabricated using InGaAs arrays [103], connected to CMOS readout electronics through a hybrid approach [104]. Alternatives based on Ge have been produced by NoblePeak and are described in [105]. The Company developed a process based on standard CMOS technology with an additional module for the growth of relatively thick Ge, due to absorption constraint for surface illuminated detectors. As imaging is more sensitive to dark current than high-speed optical communication, a "necking" technique [106] was used to reduce the number of dislocations in the film. Similar devices, although based on different methods to grow the Ge films, are reported in [107] (polycrystalline Ge) and [108] (epitaxial Ge using LEPECVD).

8.10 Reliability

In spite of the vast amount of work done on the integration of Ge films on Si for photo-detection, reports on the crucial aspect of reliability of these devices are still sparse. Luxtera has published the most extensive results on long terms aging of Si/Ge detectors in [109]. ~1200 detectors from several CMOS lots were aged under stress conditions recommended in Telcordia GR-468-CORE, which consist of biasing the detectors at twice their nominal operating voltage without incident light and aging them at 175 °C for 2000 h, while monitoring dark current. The results showed no wear-out in the dark current of the detectors (Figure 8.10) and also no sudden death failures, thereby establishing the 90% confidence random failure rate for the Si/Ge PIN detectors to be less than 1%.

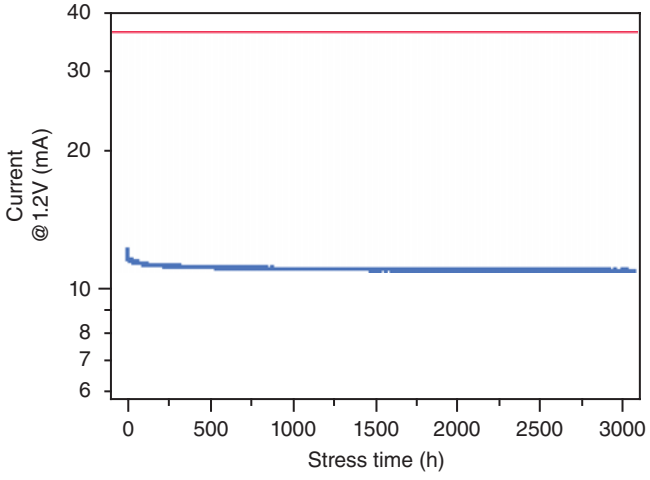


Figure 8.10 Long-term aging results for dark current at nominal bias, of a parallel array of ~200 Ge-on-Si waveguide photo-detectors [108]. Stress conditions are in accordance with Telcordia GR-468-CORE (175 °C, 2× nominal operating voltage).

8.11 Conclusions

Interest in the monolithic integration of Ge photo-detectors on Si has never been stronger. As the requirement for optical interconnects continually spreads to shorter distances, the optics industry faces fresh challenges related to the production of cost-effective and reliable high-speed optical components and sub-systems at ever higher volumes, a challenge which is well suited to the benefits offered by integration. Ge-on-Si detection technology has proved to be one of the primary enablers of this move to denser integration. Aided by the interest in Ge as a CMOS material in advanced transistor nodes, several process breakthroughs have occurred in the past decade, which, building on prior work, have allowed the production of Ge/Si detectors in several foundries around the world. Volume deployment of these detectors in commercial applications is well underway, with millions of devices already in the field in high-performance computing links. It can be expected that process technology as well as device and system design will continue to improve in the coming years as the adoption of monolithic Ge/Si detectors becomes more prevalent in the optics industry.

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9
Ge and GeSi Electroabsorption Modulators

Jifeng Liu

9.1
Introduction

Low-energy, high-speed photonic modulators on Si are important components for integrated photonics. While Si electro-optical (EO) modulators based on carrier-induced refractive index changes have achieved great success in the past decade [1–4], the trade-off between operation wavelength range and energy consumption/thermal stability is still hard to overcome [4, 5]. Conventional Mach–Zehnder interferometer (MZI) structures tend to have large footprints with high power consumption due to the limited refractive index change ($\Delta n \sim 10^{-4}$ to 10^{-3}). On the other hand, energy-efficient micro-resonator modulators have limited operation wavelength range and tend to suffer from resonant peak shifts due to thermo-optical effects.

Electroabsorption modulators (EAMs) offer much lower energy consumption than phase modulators by turning the material from transparent to opaque in the working wavelength regime under an applied electric field. The change in absorption coefficient is typically in the order of $100-1000\,\mathrm{cm}^{-1}$, which enables a very short device length in the order of $10-100\,\mu\mathrm{m}$ compared to the millimeter length scale for MZIs. The reduction in device footprint reduces the capacitance of the devices. Because the average power consumption of the modulator is $1/4\,CV_{\mathrm{pp}}^2$ in digital data links, where C is the capacitance and V_{pp} is the peak-to-peak voltage swing, a reduced capacitance leads to lower power consumption. Furthermore, the RC limited bandwidth is also increased. Because the electroabsorption is a field effect where the response time is less than a picosecond [6], the bandwidth is only limited by RC delay [7]. However, the electroabsorption effect (EAE) is only significant for direct gap transitions. The lowest direct gap transition in Si is ~3.4 eV, which is too large to apply for near infrared integrated photonics.

Ge-on-Si provides a unique opportunity for integrated EAMs. Although Ge is considered an indirect gap semiconductor, the energy difference between its direct gap at the Γ valley and indirect gap at the L valleys is only 136 meV [8], or $\sim 5\,k_{\mathrm{B}}T$ at room temperature (k_{B} is the Boltzmann constant). The direct band gap of 0.8 eV

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corresponds to a wavelength of 1550 nm, the most technically important wavelength in optical communications and the most commonly used in Si photonics so far. Ge and GeSi EAMs have been developed in the past decade based on this direct gap transition. In this chapter, we will first discuss the theory and working principles of Ge and GeSi EAMs. We will then review the waveguide-coupling schemes for integrated modulators, and finally summarize the state-of-the-art progress in this field.

9.2 EAE in Ge and GeSi: Theoretical and Experimental

Similarly to III–V semiconductors, the direct gap absorption in Ge can be effectively modified by an applied electric field, demonstrating a strong EAE. EAE in semiconductors include the Franz–Keldysh effect (FKE) in bulk materials and the quantum-confined Stark effect (QCSE) in quantum well (QW) structures. We will discuss these two effects specifically for Ge and Ge-rich GeSi alloys in this section.

9.2.1 Franz–Keldysh Effect

Figure 9.1a,b schematically shows the optical absorption process and absorption spectra in a semiconductor material with and without an electric field. Without the field, photons with energy less than the band gap are not absorbed, while those with energy above the band gap are (Figure 9.1a). The absorption coefficient spectrum follows the well-known square-root relation for direct gap transitions, that is, proportional to the joint density of states (Figure 9.1c, dashed line). With an applied field, the absorption process can be considered as band-to-band tunneling under photon excitation. In this case, even a photon with $h\nu < E_g$ can excite an electron from the valence band to the conduction band through a cooperative tunneling process across a triangular energy barrier (Figure 9.1b). Therefore, the absorption coefficient at $h\nu < E_g$ increases compared to the case without the electric field (Figure 9.1c, solid line). On the other hand, for $h\nu$ slightly greater than E_g the absorption curve shows oscillating behavior near the band edge, known as Franz–Keldysh oscillations (Figure 9.1c, solid line). This is because for excited electrons with energy slightly greater than the triangular barrier, the probability to cross the barrier and reach its final state on the tilted conduction band edge is determined by the interference between the electron wavefunction and the barrier. This phenomenon is well known in quantum tunneling and it is similar to the Fabry–Perot oscillations in optics, both resulting from the nature of waves. As a reminder, Figure 9.1d shows the transmission probability through a rectangular potential barrier with a height of $V_0 = 0.1$ eV and a width of 4.5 nm as a function of the electron energy normalized to V_0. The finite tunneling probability at $E < V_0$ and oscillations at $E > V_0$ closely resemble the features of the absorption spectrum under an electric field in Figure 9.1c. While the picture presented above is simplified, it does capture most of the physics in FKE [10].

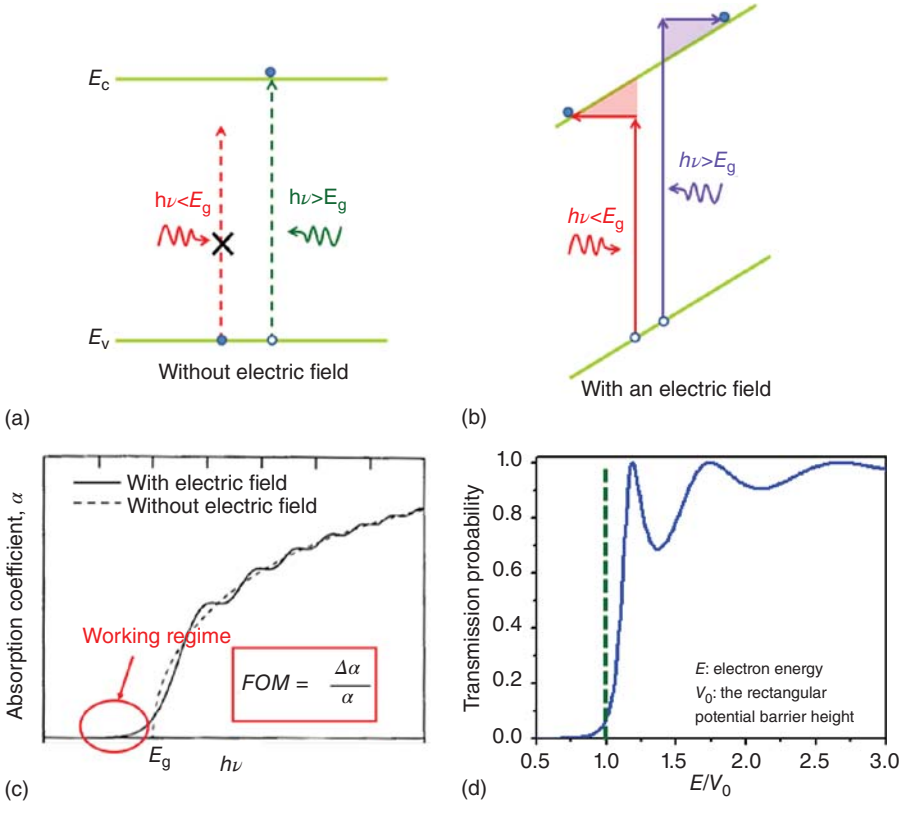

Figure 9.1 (a) Schematics of band-to-band optical absorption in a bulk semiconductor material without an applied electric field. (b) Schematics of absorption process in a bulk semiconductor material under an applied electric field (Franz–Keldysh effect). (c) Corresponding absorption spectra of the bulk semiconductor material with and without an electric field. (d) The transmission probability through a rectangular potential barrier with a height of $V_0 = 0.1$ eV and a width of 4.5 nm as a function of the electron energy normalized to V_0. The finite tunneling probability at $E < V_0$ and oscillations at $E > V_0$ closely resemble the features of the absorption spectrum under an electric field in (c). Panels (a)–(c) are reproduced from Ref. [9] with permission under MDPI's Creative Commons Attribution License.

The figure-of-merit (FOM) for EAM materials and devices is the absorption contrast, $\Delta\alpha/\alpha$, that is, the relative change in absorption coefficient when an electric field is applied. As shown in Figure 9.1c, this FOM is maximized at photon energies slightly smaller than the direct band gap.

A rigorous analysis of the FKE can be obtained by solving the Schrödinger's equation of an electron-hole pair in the presence of an electric field F applied along the z-direction [11]:

$$\left(-\frac{\hbar^2}{2m_r}\frac{d^2}{dz^2} + eFz\right)\varphi(z) = E_z\varphi(z), \tag{9.1}$$

where $m_r = m_e m_h/(m_e + m_h)$ is the reduced effective mass of electrons and holes. The total energy E is given by

$$E = \frac{\hbar^2}{2m_r}(k_x^2 + k_y^2) + E_z. \tag{9.2}$$

The solution to this equations is given by

$$\varphi_{E_z}(z) = \left(\frac{2m_r}{\hbar^2}\right)^{1/3} \frac{1}{(eF)^{1/6}} Ai\left[\left(\frac{2m_r eF}{\hbar^2}\right)^{1/3}\left(z - \frac{E_z}{eF}\right)\right], \tag{9.3}$$

where Ai(Z) is the Airy function, which is now available in most mathematic software (e.g., Matlab). Applying Fermi's Golden Rule and integrating over all available quantum states of k_x, k_y, and E_z upon a photon excitation of $h\nu$, we can obtain the absorption coefficient $\alpha(h\nu, F)$ of the direct gap transition under the applied electric field F:

$$\alpha(h\nu, F) = \frac{e^2 E_p}{24\pi n_r c\varepsilon_0 m_0 \nu}\left\{\left(\frac{2m_{r,lh}}{\hbar^2}\right)^{3/2}\sqrt{\hbar\theta_{F,lh}}[-\eta_{lh}Ai^2(\eta_{lh}) + Ai'^2(\eta_{lh})]\right.$$
$$\left. + \left(\frac{2m_{r,hh}}{\hbar^2}\right)^{3/2}\sqrt{\hbar\theta_{F,hh}}[-\eta_{hh}Ai^2(\eta_{hh}) + Ai'^2(\eta_{hh})]\right\},$$

where $m_{r,lh} = m_e^{\Gamma} m_{lh}/(m_e + m_{lh})$, $m_{r,hh} = m_e^{\Gamma} m_{hh}/(m_e + m_{hh})$, $\hbar\theta_{F,lh} = ((\hbar^2 e^2 F^2)/2m_{r,lh})^{1/3}$, $\eta_{lh} = (E_g^{\Gamma,lh} - h\nu)/\hbar\theta_{F,lh}$,

$$\hbar\theta_{F,hh} = \left(\frac{\hbar^2 e^2 F^2}{2m_{r,hh}}\right)^{1/3} \quad \text{and} \quad \eta_{hh} = \frac{E_g^{\Gamma,hh} - h\nu}{\hbar\theta_{F,hh}}. \tag{9.4}$$

Equation (9.4) takes into account the transitions from both light hole and heavy hole bands, considering that they have different effective mass and that the band gaps $E_g^{\Gamma,hh}$ and $E_g^{\Gamma,lh}$ can be different when strain is introduced to the materials. Thermally induced tensile strain in Ge-on-Si reduces the energy difference between the direct and indirect gaps [12–17]. The material constants of 0.2% tensile strained Ge-on-Si are: band-to-band transition matrix element $E_P = 26.3\,\text{eV}$, the direct gap associated with light hole band $E_g^{\Gamma,lh} = 0.773\,\text{eV}$, the direct gap associated with the heavy hole band $E_g^{\Gamma,hh} = 0.785\,\text{eV}$, the effective mass of electrons in the direct Γ valley $m_e^{\Gamma} = 0.038m_0$, the light hole effective mass $m_{lh} = 0.043m_0$, and the heavy hole effective mass $m_{hh} = 0.33m_0$ [8]. In Eq. (9.4), n_r is the refractive index (wavelength dependent); c is the speed of light in vacuum; ε_0 is the dielectric constant of vacuum; m_0 is the mass of an electron; e is the electron charge; $\hbar$ is the Planck's constant divided by 2π; and Ai' is the derivative of the Airy function.

The FKE of the indirect gap is three orders of magnitude lower than that of the direct gap and can be neglected in the modeling [18, 19]. On the other hand, the contribution of the indirect gap absorption to the overall absorption coefficients is not negligible. The indirect gap absorption of Ge can be obtained by interpolating and extrapolating the experimental data for the indirect gap transition reported by Dash and Newman [20]. The total absorption coefficient is

a sum of the contributions from the direct and indirect band gaps of Ge [7]. Based on this consideration, we can also see that the smaller the difference between the direct and indirect gap, the larger the absorption contrast $\Delta\alpha/\alpha$. As tensile strain reduces such an energy difference, it enhances the FKE in Ge and GeSi, as will be discussed later in more detail.

To blue-shift the optimal operation wavelength to $\lambda \sim 1550\,\text{nm}$, a few atomic percent of Si is often alloyed with Ge. In this case the material parameters in Eq. (9.4) needs to be modified to those of GeSi alloys. Note that although the minimal direct gap of Si is 3.4 eV, this is actually due to the cross-over of two conduction bands at $k = 0$, which is often referred to as E'_0 or Γ_{15}. The fundamental direct gap of Si is $E_0 = 4.06\,\text{eV}$ (known as Γ_{25}) at room temperature [21]. Therefore, the linearly interpolated direct band gap of unstrained $Ge_{1-x}Si_x$ is

$$E_g^{\Gamma}(Ge_{1-x}Si_x) = (0.8 + 3.26x)\,\text{eV}. \tag{9.5}$$

Such linear interpolations work well for GeSi mainly because Ge and Si form a complete solid solution. To take into account the effect of strain on the direct gap, one can also linearly interpolate the deformation potentials, the elastic constants, and split-off energy [8, 14, 22, 23]. The deformation potential constants are given by: $a(Ge_{1-x}Si_x) = -(8.97 - 3.87x)\,\text{eV}$, $b(Ge_{1-x}Si_x) = -(1.88 + 0.32x)\,\text{eV}$, and $d(Ge_{1-x}Si_x) = -(4.7 + 0.1x)\,\text{eV}$. The elastic constants of $Ge_{1-x}Si_x$ are given by $C_{11}(Ge_{1-x}Si_x) = (128.53 + 37.27x)\,\text{eV}$, $C_{12}(Ge_{1-x}Si_x) = (48.26 + 15.64x)\,\text{eV}$, $C_{44}(Ge_{1-x}Si_x) = (66.80 + 12.80x)\,\text{eV}$.The split-off energy is given by $\Delta_0(Ge_{1-x}Si_x) = 0.29 - 0.246x$. Further referring to Chapters 10 and 12 of this book, the band gaps from the maxima of light hole, heavy hole, and split-off bands to the minimum of the Γ valley, that is, $E_g^{\Gamma,lh}$, $E_g^{\Gamma,hh}$, and $E_g^{\Gamma,\text{so}}$, can be calculated. With the approach described above, the direct band gap of the $Ge_{1-x}Si_x$ material can be obtained given the composition and the strain.

The indirect gap of GeSi as a function of Si composition for $x < 0.15$ is given by [24]

$$E_g^{L}(Ge_{1-x}Si_x) = (1.86 - 1.2x)\,\text{eV}. \tag{9.6}$$

The indirect gap absorption for $x < 0.03$ can be approximated by blue-shifting the indirect absorption spectrum reported in [20] to the indirect gaps of $Ge_{1-x}Si_x$. From Eqs (9.5) and (9.6), we can also see that the energy difference between the direct and indirect gaps increases with Si content x. This will lead to a higher background indirect gap absorption loss and reduce $\Delta\alpha/\alpha$.

The effective mass of electrons and holes of $Ge_{1-x}Si_x$ is almost the same as Ge for $x < 0.03$, and the difference is actually within the experimental error [8]. Therefore, we simply use the electron and hole effective mass of Ge in our simulation for $Ge_{1-x}Si_x$ with $x < 0.03$. From the $k \cdot p$ theory, the optical transition matrix element is given by [25]

$$E_P = 3(m_0/m_e^{\Gamma} + 1)/(1/E_g^{\Gamma,lh} + 1/E_g^{\Gamma,hh} + 1/E_g^{\Gamma,\text{so}}). \tag{9.7}$$

Finally, the real part of the refractive index of $Ge_{1-x}Si_x$ at 1550 nm is $n_r(Ge_{1-x}Si_x) = 4.10 - 0.64x$ [8, 24].

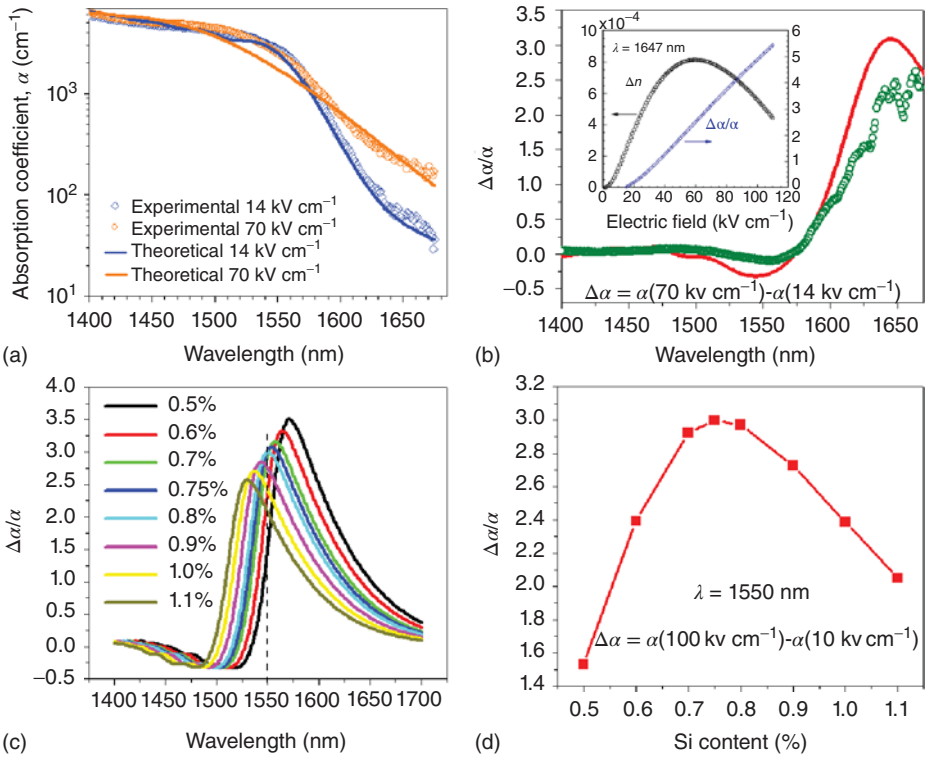

Figure 9.2 (a) Experimental and theoretical absorption spectra of 0.2% tensile strained Ge-on-Si under applied electric fields of 14 and 70 kV cm^{-1}. (b) Experimental and theoretical absorption contrast spectra (corresponding to (a)) for 0.2% tensile strained Ge-on-Si. The inset shows the calculated refractive index change Δn and absorption contrast $\Delta\alpha/\alpha$ at $\lambda = 1647$ nm as a function of applied electric field. Reproduced with permission from Ref. [26]. Copyright 2006 AIP LLC. (c) Absorption contrast, $\Delta\alpha/\alpha$, as a function of wavelength for GeSi alloys with different Si compositions. The GeSi is 0.26% uniaxially strained along the <110> direction. (d) $\Delta\alpha/\alpha$ at $\lambda = 1550$ nm as a function of Si composition. In (c) and (d) we assumed an applied electric field of 100 kV cm^{-1} and a built-in field of 10 kV cm^{-1} at 0 V in the intrinsic GeSi region. Panel (d) is reproduced from Ref. [7] under the Author's Copyright Transfer Agreement with OSA.

Using the materials parameters discussed above, one can readily model the FKE in $Ge_{1-x}Si_x$ with $x < 0.03$. While FKE in bulk Ge only shows a $\Delta\alpha/\alpha \sim 1$ [18] mainly limited by the background indirect gap transition, it turns out that 0.2% tensile-strained Ge demonstrates a significantly better absorption contrast because the energy difference between direct and indirect gaps is decreased [26]. Figure 9.2a shows the calculated absorption spectra of 0.2% tensile strained Ge-on-Si under an applied electric field of 14 and 70 kV cm^{-1}, respectively, and compares them to the experimental data derived from the responsivity spectra of Ge/Si p–i–n photodetectors. The theoretical predictions agree well with

the experimental data at photon energies slightly smaller than the direct band gap (i.e., $\lambda > 1600\,\text{nm}$). The $70\,\text{kV cm}^{-1}$ data show some deviation at photon energies slightly higher than the band gap mainly because Eq. (9.4) does not take into account the exciton effect. This omission does not pose an issue in a practical device design, though, as this photon energy regime is not of significant interest for EAM applications due to the low $\Delta\alpha/\alpha$. Figure 9.2b shows that the calculated $\Delta\alpha/\alpha$ curve agrees very well with the experimental data, with an optimal $\Delta\alpha/\alpha \sim 3$ at $\lambda = 1647\,\text{nm}$ for $F = 70\,\text{kV cm}^{-1}$. Based on the same model, the inset of Figure 9.2b further shows that $\Delta\alpha/\alpha$ can exceed 4 at $F = 85\,\text{kV cm}^{-1}$, and 5 at $F = 105\,\text{kV cm}^{-1}$. Because the breakdown field of Ge is $120\,\text{kV cm}^{-1}$ [27], these high absorption contrasts can be readily achieved by increasing the reverse bias of a Ge p–i–n diode structure. It is noteworthy that the real part of the refractive index also changes notably under an applied field (denoted by "Δn" in the inset of Figure 9.2b) due to the Kramers–Kronig relation. The EO coefficient, $\Delta n/F$, is as high as $280\,\text{pm V}^{-1}$ for $F < 50\,\text{kV cm}^{-1}$ at $\lambda = 1647\,\text{nm}$, compared to $240\,\text{pm V}^{-1}$ for InP and $164\,\text{pm V}^{-1}$ for $LiNbO_3$. The application of Ge as a field-induced EO modulator is limited by the background absorption from the indirect gap transition, though [28].

To achieve optimal absorption contrast at 1550 nm, the most technically important wavelength in optical communications, tensile strained Ge can be alloyed with a small amount of Si to increase the direct band gap of FKE modulators [7]. One should note that the addition of Si tends to decrease $\Delta\alpha/\alpha$ as it increases the difference between the direct and indirect gaps (Figure 9.2c). Nevertheless, a $\Delta\alpha/\alpha$ of ~3 can still be achieved at $\lambda \sim 1550\,\text{nm}$ (Figure 9.2d) based on the calculations described above. Such a contrast is high enough for integrated photonic devices, as will be discussed in Section 9.4.

9.2.2
Quantum-Confined Stark Effect

Figure 9.3 schematically shows the band diagrams and wavefunctions in a QW structure with and without an applied electric field. The fundamental mechanism of QCSE is similar to FKE, that is, band-to-band tunneling under photon excitation. However, there are several distinct features associated with QCSE compared to FKE:

1) In QWs, the binding energy of excitons is notably larger than in bulk materials due to the quantum confinement, where a pair of electron and hole is pushed closer to each other. As a result, the strong exciton absorption peaks are clearly visible even at room temperature (Figure 9.3b, [29]). Therefore, in addition to band-to-band transitions, the significant exciton absorption peak and its shift with applied electric field will notably enhance the EAE compared to bulk materials.
2) In QCSE the absorption spectrum redshifts under the applied electric field, while in FKE it looks more like a band edge tilt toward lower photon energy.

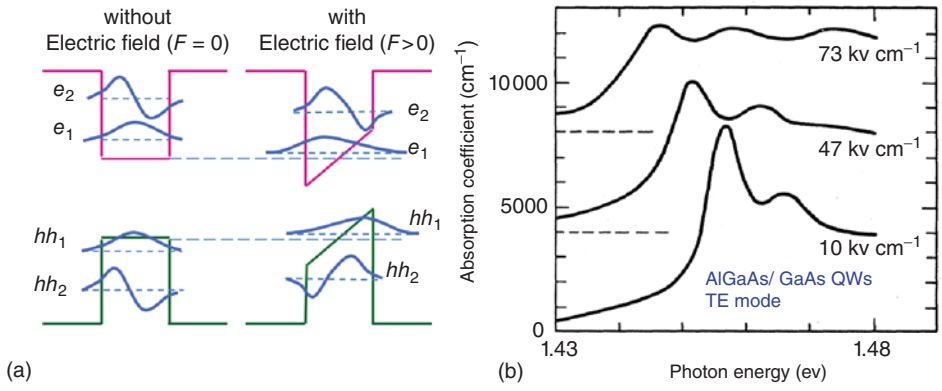

Figure 9.3 (a) Schematic band diagrams and wavefunctions of QW structures without (left) and with (right) an applied electric field. Here electron (e_1, e_2) and heavy hole (*hh*1, *hh*2) wavefunctions are shown. The electric field redshifts the energy levels and distort the wavefunctions in the QWs. Together with the redshift of the exciton absorption peaks, the absorption spectrum is redshifted under an applied field, as shown in (b). In this case an example of AlGaAs/GaAs QWs is shown. The light is polarized within the plane of the QW structure. The peaks in the figure correspond to exciton absorption. The dashed lines show the baselines for the two upper curves. Reproduced from Ref. [29] with permission from American Physical Society.

This feature is due to the redshift of the *discrete* exciton peaks and the *discrete* sub-bands of the QWs.

3) The peak absorption coefficient in the spectra decreases as the applied field increases. As shown in Figure 9.3a, this phenomenon is because the electron and hole wavefunctions have less overlap under an applied field. That is, the electrons tend to move to the lowest energy corner in the conduction band on one side of the QW, while the holes tend to move to the highest energy corner in the valence band at the other corner. In addition, the electric field tends to dissociate the excitons. Therefore, the exciton peaks become weaker and broader under an applied field.

4) The transverse electric (TE, polarized parallel to the plane of the QWs) and transverse magnetic (TM, polarized perpendicular to the QW) polarizations behave differently in QCSE due to the QW structure. In highly strained bulk semiconductors, polarization dependence of EAE can also occur due to the different transitions from *lh* and *hh* bands. However, for 0.2% tensile strained Ge and GeSi this effect is weak. For QWs, on the other hand, the polarization dependence cannot be neglected because the layered QW structure itself breaks the cubic symmetry in the direction perpendicular to the QWs. Due to the selection rules, under TE mode the $hh \rightarrow \Gamma$ valley absorption is three times stronger than that from *lh*. Under TM mode, the $hh \rightarrow \Gamma$ transition is forbidden and the $lh \rightarrow \Gamma$ transition is three times stronger than the TE mode [30]. In integrated photonics, TE mode is usually preferred due to a higher optical confinement.

For quantitative modeling of QCSE, the readers are referred to [11, 29] because the derivations are too lengthy to incorporate into this chapter. For the case of SiGe/Ge QWs, the fundamental material parameters for Ge and SiGe can be found in Section 9.2.1 and related references. Reiger and Vogl [31] evaluated the alignment of the valence band and the indirect conduction valley for Type I QW structures in SiGe/Ge QW design. For relaxed $Si_{1-x}Ge_x$ grown on $Si_{1-y}Ge_y$ substrate or barrier layer, the valence band offset (averaged over *lh*, *hh*, and split-off bands) is given by

$$\Delta_{av} = E_v(Si_{1-x}Ge_x) - E_v(Si_{1-y}Ge_y) = (0.47 - 0.06y)(x - y)\,\text{eV} \tag{9.8}$$

Further considering the band gaps of SiGe alloys given by Eqs (9.5) and (9.6), one can easily find out the conduction band offset accordingly. For strained SiGe alloys, we can use Eq. (9.8) as the baseline and apply deformation potential theory (Chapter 10 of this book, [14, 23, 31]) and corresponding materials parameters discussed in Section 9.2.1 to obtain the band offsets. As an example, the conduction and valence band offsets of pseudomorphic (lattice matched) $Si_{1-x}Ge_x$ grown on <001> $Si_{1-y}Ge_y$ is shown in Figure 9.4. According to the definition labeled in the figures, a negative band offset in the conduction band and a positive offset in the valence band indicates Type-I alignment. One can find that Type I alignment can be achieved for Ge-rich GeSi with $0.75 \leq x \leq 1$ grown on a barrier layer of $0.6 \leq y \leq 1$. In particular, Ge QW grown on $Si_{0.15}Ge_{0.85}$ barrier layers shows a conduction band offset of −0.13 eV and a valence band offset of 0.10 eV, providing quantum confinement for both electrons and holes.

Kuo *et al.* [32] reported the first observation of strong QCSE in Ge QWs. The composition of the barrier layers was $Si_{0.15}Ge_{0.85}$ based on the proposal from [31], as mentioned earlier. Figure 9.5a shows the band diagram of the QW structure, where Type I alignment for both the direct and indirect conduction valleys are

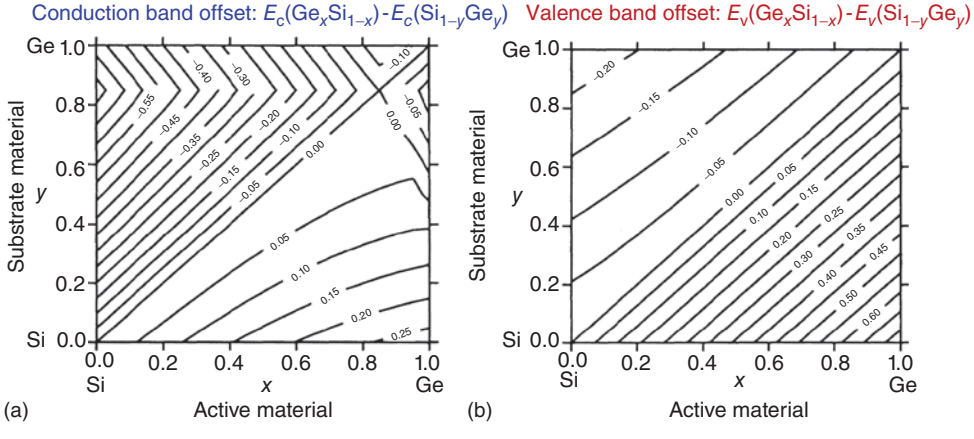

Figure 9.4 (a) Conduction and (b) valence band offsets of pseudomorphic (lattice matched) $Si_{1-x}Ge_x$ grown on <001> $Si_{1-y}Ge_y$. Reproduced from Ref. [31] with the permission from the American Physical Society.

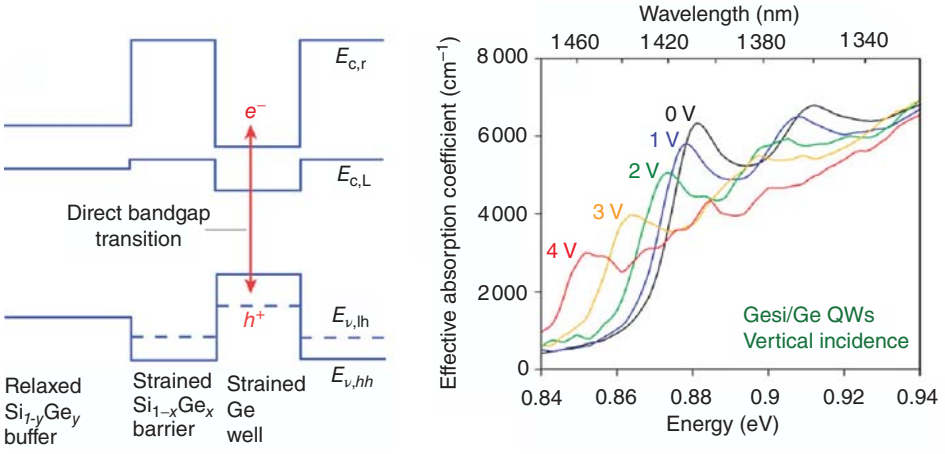

Figure 9.5 (a) Band diagram of a 10 nm Ge/16 nm $Si_{0.15}Ge_{0.85}$ QW structure. (b) Absorption spectra at different reserve biases demonstrating strong QCSE from the direct gap transition of Ge. Here 3 V reverse bias corresponds to an electric field of ~80 kV cm^{-1}. Reprinted by permission from Macmillan Publishers Ltd: NATURE [32], copyright (2005).

obtained. The band-offset in the direct Γ valley was as large as 0.4 eV, providing strong confinement for the demonstration of QCSE in Ge QWs. The multiple QW (MQW) structure was grown on a relaxed $Si_{0.1}Ge_{0.9}$ buffer layer on Si, and a vertical p–i–n diode structure was fabricated. The electroabsorption spectra was derived by measuring the responsivity spectra of the device at different reverse biases under vertical incidence, similar to [26] in measuring FKE from tensile strained Ge. As shown in Figure 9.5b, clear exciton absorption peaks and redshift in absorption spectra were observed as the reserve bias increased from 0 to −4 V, similarly to the behavior of direct gap AlGaAs/GaAs QWs in Figure 9.3b. Here −3 V reverse bias corresponded to an electric field of ~80 kV cm^{-1}, and −4 V corresponded to ~105 kV cm^{-1}. The maximum absorption contrast $\Delta\alpha/\alpha$ is ~4.7 at 1461 nm under −4 V reverse bias. This is mainly limited by the background absorption from the indirect gap transition of Ge.

There are several approaches to redshift the operation wavelength to $\lambda \sim 1550$ nm for SiGe/Ge QCSE modulators with a direct band gap corresponding to $\lambda \sim 1430$ nm. One could heat up the device (e.g., 100 °C) to reduce the band gap [33], Figure 9.6a, apply a larger electric field to extend the QCSE spectral regime [34], Figure 9.6b, or utilize some strain engineering approaches (see Chapters 10 and 12) to convert the compressive strain in the Ge QWs into *tensile* strain. Tensile strain engineering is the most favorable method as it avoids additional power consumption induced by heating or increased reserve bias. It also helps to reduce the energy difference between the direct and indirect gaps in Ge QWs, thereby increasing $\Delta\alpha/\alpha$. Although tensile strained Ge QW structures have been reported before [35, 36], the QCSE effect has not been studied in these

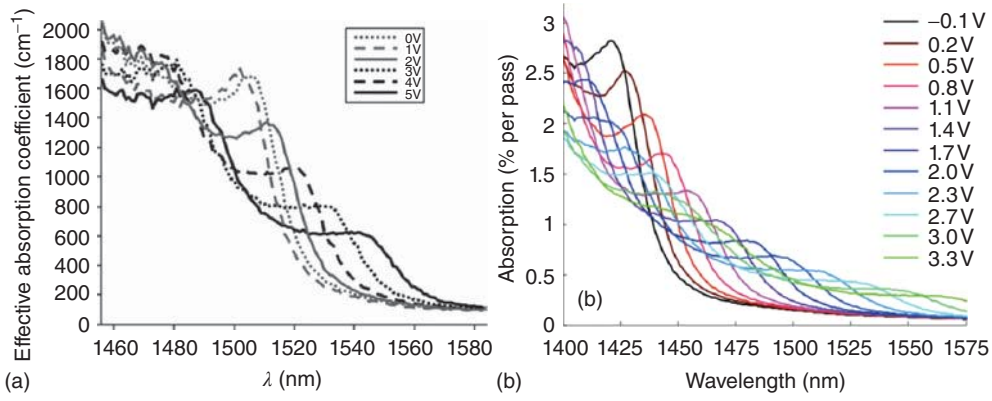

Figure 9.6 C band ($\lambda = 1520 - 1560$ nm) Ge QCSE achieved by (a) heating the device to 100 °C. Reproduced from Ref. [33] with the permission from the Institution of Engineering and Technology. (b) Improving the QW design and applying a large enough electric field to extend the electroabsorption edge into longer wavelengths. In this case a 12 nm Ge/17 nm $Si_{0.19}Ge_{0.81}$ MQW structure is adopted. © 2013 OSA Reproduced from Ref. [34].

structures. On the other hand, broad-band QCSE effect has been demonstrated recently by improving the QW design and controlling the DC reverse bias during operation [34]. Different from previous QW structures, the 0.18% thermally induced tensile strain in the SiGe buffer layer was taken into account to design the QW stack. The Si composition in the buffer layer was increased from 10% to 12% to further reduce the lattice mismatch with the Si substrate, and the QW stack is designed to have an average lattice constant identical to the tensile strained $Si_{0.12}Ge_{0.88}$ buffer layer. The Si composition in the barrier layers was increased from 15% to 19% correspondingly. This design enabled thin buffer layers and Ge QW stacks such that the same electric field can be achieved at a lower reverse bias compared to the original structure in [32]. By measuring the responsivity spectra versus reverse bias of a vertically incident Ge QW p–i–n photodiode, it was found that the absorption edge can be shifted beyond 1550 nm at −3.3 V reverse bias (Figure 9.6b). A $\Delta\alpha/\alpha$ of ~3.5 can be achieved at a voltage swing of $V_{pp} = 1$ V in S band and C band by increasing the reverse DC offset from −0.4 to −3 V. Based on the materials performance, it was predicted that a 200 μm-long waveguide-coupled Ge QW device can achieve 6.5 dB extinction ratio/4 dB insertion loss and 15 dB extinction ratio/7 dB insertion loss at 1550 and 1490 nm, respectively.

The operation wavelength of Ge QCSE can also be blue-shifted. Very recently, a Ge QCSE modulator with 8 nm Ge/12 nm $Si_{0.35}Ge_{0.65}$ barrier layers working at 1300 nm has been reported, covering another important wavelength in optical communications [37]. Figure 9.7a schematically shows the device structure. The increased Si content in the barrier layer provides stronger quantum confinement that further increases the direct band gap of the Ge QWs for operation near 1300 nm. Figure 9.7b shows the electroabsorption spectra of the device under TE

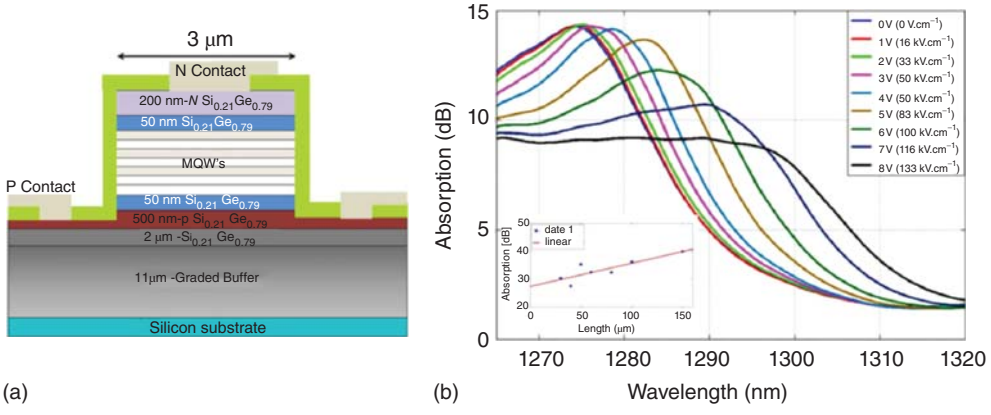

Figure 9.7 (a) Schematic cross-section of a Ge QCSE modulator operating around $\lambda = 1300$ nm. The active region consists of 20 pairs of 8 nm Ge/12 nm $Si_{0.35}Ge_{0.65}$ MQW structures (b) Electroabsorption spectra of the device under different reverse biases for TE polarization. The inset shows the absorption as a function of the length of the device (cut back method) to determine and remove the coupling loss from the fiber into and out of the device. © 2014 IEEE Reprinted, with permission, from Ref. [37].

polarization using a lensed-fiber for butt-coupling. The extinction ratio can reach 6 dB with an insertion loss of 2.5 dB at $\lambda = 1293$ nm.

9.2.3
Comparison of Ge FKE with QCSE Modulators

In III–V materials, typically, QCSE shows a much stronger absorption contrast than FKE mainly due to the additional contribution from excitons induced by quantum confinement. In the case of Ge, QCSE indeed shows a much larger $\Delta\alpha$ compared to FKE at the same electric field of ~100 kV cm^{-1}, that is, $\Delta\alpha \sim 2500$ cm^{-1} at 1461 nm versus ~300 cm^{-1} at 1647 nm (see Figures 9.2a,b and 9.5b). However, two factors work against high absorption contrast($\Delta\alpha/\alpha$) in Ge QCSE. (i) The quantum confinement effect itself *increases* the energy difference between the direct and indirect gaps of the Ge QWs. As shown in Figure 9.5a, electrons in the direct Γ valley see a much deeper well compared to those in the indirect L valleys, and their effective mass is much smaller than that in L valleys (0.038 m_0 vs. 0.2 m_0). Therefore, the energy levels of the direct Γ valley increase more dramatically than those of the indirect L valleys upon quantum confinement, and the Ge QW becomes more of an indirect gap semiconductor. (ii) The *compressive* strain in SiGe/Ge QWs due to the lattice mismatch between Ge and $Si_{0.15}Ge_{0.85}$ also increases the energy difference between the direct and indirect gaps. Consequently, the background absorption loss from the indirect gap transition of Ge QWs is also significantly higher than that of 0.2% tensile strained bulk Ge (500 cm^{-1} vs. 60 cm^{-1}).Overall, the $\Delta\alpha/\alpha$ of QCSE in Ge QWs is similar to that of FKE in tensile strained Ge under the same applied electric

field of ~100 kV cm^{-1}, although the optimal working wavelengths are different (1461 nm vs. 1647 nm). Considering that the absorption contrasts are comparable while a single tensile-strained Ge epitaxial layer is much easier to grow than multiple Ge QWs, for integration with complementary metal oxide semiconductor (CMOS) process it is more convenient to use tensile-strained enhanced FKE for waveguide-coupled Ge EAMs. Moreover, the optical confinement in Ge and GeSi FKE modulators is typically larger than that in the Ge QWs.

On the other hand, due to the large $\Delta\alpha$ in QCSE, these devices can potentially achieve the same extinction ratio with a shorter device length, thereby consuming less power than the FKE devices. These will be discussed in more detail in Section 9.4.

In terms of operation wavelength range, FKE of tensile strained Ge and GeSi can easily cover the C band (1520–1560 nm) and L band (1561–1630 nm) due to the adequate band gaps, as shown in Figure 9.2. It is difficult to push the operation range to 1310 nm as it requires more Si alloying to increase the band gap, yet doing so will decrease the $\Delta\alpha/\alpha$ as mentioned in Section 9.2.1. By comparison, QCSE in Ge QWs is more suitable for shorter wavelengths ≤1550 nm, as shown in Figures 9.6 and 9.7. It is relatively easy to push the operation wavelength range to 1310 nm by increasing the Si content in the barrier layer without changing the Ge QW itself. As mentioned earlier, a drawback is that the stronger quantum confinement and higher compressive strain also increases the energy difference between the direct and indirect gaps, thereby reducing $\Delta\alpha/\alpha$. In both cases, tensile strain engineering will help to drive the material toward a direct gap semiconductor and enhance the absorption contrast mainly be reducing the background absorption loss from the indirect gap transitions. Recently developed tensile strain engineering methods [38, 39] could potentially be applied to Ge and GeSi EAMs to enhance their performance.

9.3 Waveguide Coupling

For photonic integration on Si, waveguide-coupling with Ge and GeSi EAMs is indispensable in the construction of photonic circuits. Because light has to be coupled efficiently *into and out* of the modulators, butt-coupling has been the most popular approach to achieve high coupling efficiency. Evanescent coupling has also been demonstrated in recent years, yet the insertion loss tends to be high because the light tends to be confined in the high index Ge or GeSi materials.

Butt-coupling launches optical power directly into the Ge or GeSi active device region from one end, and couples out the modulated optical signal from the other end (Figure 9.8, [40]). Thus, it offers a higher coupling efficiency compared to evanescent coupling in most cases. The same butt-coupling structure can be applied to all Ge active photonic devices for monolithic photonic data links [7, 41]. The fabrication process of butt-coupled devices is typically more elaborate than evanescently coupled ones, though, because Ge has to be selectively grown

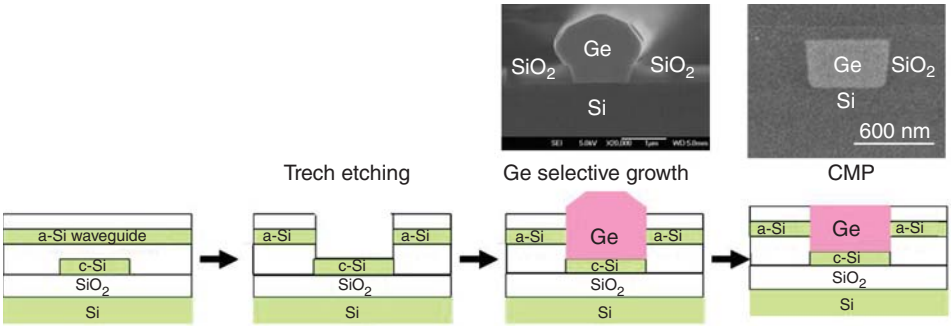

Figure 9.8 Schematic fabrication process of butt-coupled Ge EAMs on silicon-on-insulator (SOI) platform. "a-Si" and "c-Si" refer to amorphous Si and crystalline Si, respectively. Trench-filling selective growth is applied to achieve these structures. Cross-sectional SEM pictures of trench-filled Ge selective growth and the Ge region after CMP are also shown. © 2006 IEEE. Reprinted, with permission, from [40].

to fill pre-defined trenches in order to implement butt-coupling structures [42–44]. Chemical mechanical polishing (CMP) is often required to flatten the top of the Ge mesas because single crystalline selective growth usually results in faceting and a non-planar surface [45]. An example of such a fabrication process is schematically shown in Figure 9.8, where cross-sectional scanning electron microscopy (SEM) images of Ge overgrown out of the trench and after planarization are also presented. To prevent Ge growth on the exposed end of amorphous Si (a-Si), one can also deliberately leave an oxide or nitride spacer at the end of the a-Si waveguides [42, 43]. Ge does not grow on oxide or nitrides during selective growth.

Several types of butt-coupling structures have demonstrated high coupling efficiencies. For example, the Ge EAM has been designed and fabricated as a segment of the waveguide, with its dimensions optimized for maximum modal overlap with that of the input and output Si waveguides [7, 41, 42]. Figure 9.9a shows such a design, in which the light is first coupled vertically from a crystalline Si (c-Si) waveguide to a short segment of a-Si waveguide, then butt-coupled from the a-Si waveguide to the GeSi region. The reason for such a configuration is that the a-Si waveguide is more lossy than c-Si so that one would use c-Si waveguide as much as possible to minimize the propagation loss. The corresponding c-Si to a-Si tapered vertical coupler design can be found in [46]. The dimensions of GeSi waveguide is optimized by considering the trade-off between the modal overlap with the a-Si waveguide and the optical confinement factor in the GeSi region (Figure 9.9b), as well as the tolerance to fabrication errors. The coupling loss, including both input and output coupling, is theoretically predicted to be 1 dB [7] compared to the experimentally estimated coupling loss of 1.6 dB [41]. Details of the design are discussed in [7].

In another butt-coupling design, Feng *et al.* [44, 47] use tapered mode converters to enhance the butt-coupling efficiency between Si and GeSi ridge waveguides (Figure 9.10). This mode-converter butt-coupling design is especially useful when

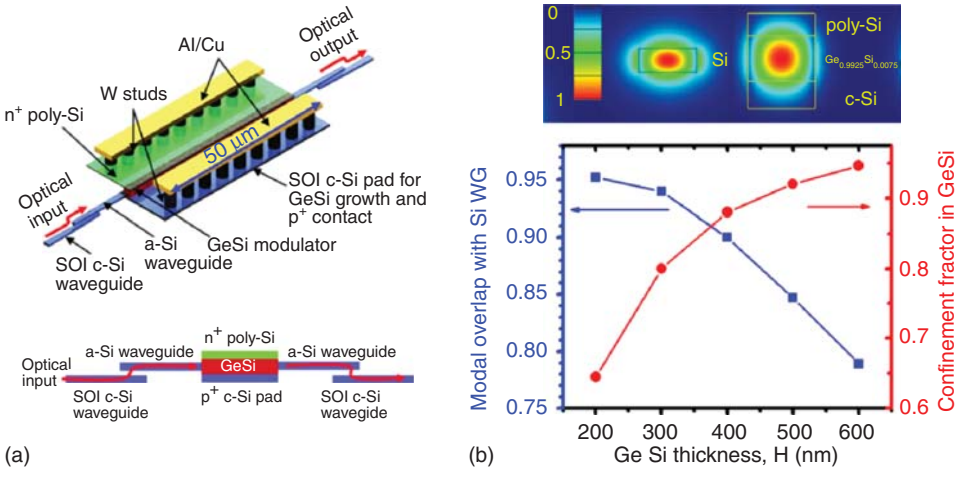

Figure 9.9 (a) Schematics of waveguide-coupled GeSi EAM (based on FKE). The upper part shows a 3D cartoon, while the lower part shows the longitudinal cross-section. Reprinted from Ref. [41] under the Author's Copyright Agreement with Nature Publishing Group. (b) Upper part: TE mode profiles in the Si waveguide versus the GeSi EAM. The Si waveguide has a cross-section of 500 nm × 200 nm, while the GeSi active region is 600 nm × 400 nm with 200 nm Si on top and bottom. Lower part: Modal overlap with the Si waveguide and optical confinement factor in the GeSi region as a function of GeSi layer thickness. The width of the GeSi region is fixed at 600 nm. Reproduced from Ref. [7] under the Author's Copyright Transfer Agreement with OSA.

there is a large mismatch between the cross-sectional dimensions of input waveguide and the GeSi region. As shown in Figure 9.10b,c, with the mode conversion the optical mode profile in the Si waveguide is remarkably similar to that in the Ge EAM region right before coupling, and the theoretically calculated coupling loss is as low as 0.15 dB. Experimentally, a coupling loss of ~1.3 dB was demonstrated mainly limited by the fabrication error.

The butt-coupling scheme has also been applied to Ge QCSE modulators [48]. A challenge in this case, though, is that there is a big mismatch in the mode profile between the Si waveguide and the Ge QCSE region. The Si waveguide is 300 nm thick, while the Ge/GeSi region is as thick as 1.5 μm. As a result, simulations show a 12 dB coupling loss compared to 15 dB measured experimentally. Ren *et al.* [48] suggested that this excess loss could be alleviated by starting with a selective regrowth of Si to reduce the required thickness of SiGe growth. In view of Figure 9.10, another possibility is to use tall Si ridge waveguides instead of flat Si channel waveguides for coupling into the Ge QCSE modulator region. In principle, the coupling loss could be as low as the cases for Ge FKE modulators with optimal design and fabrication.

It is also noteworthy that Vivien *et al.* [49] used a wide patch of Ge to capture the optical power coupled and scattered into the Ge region for high efficiency waveguide-coupled photodetectors. This kind of optical design is somewhat similar to multi-mode interference (MMI) couplers. It could be extended to MMI

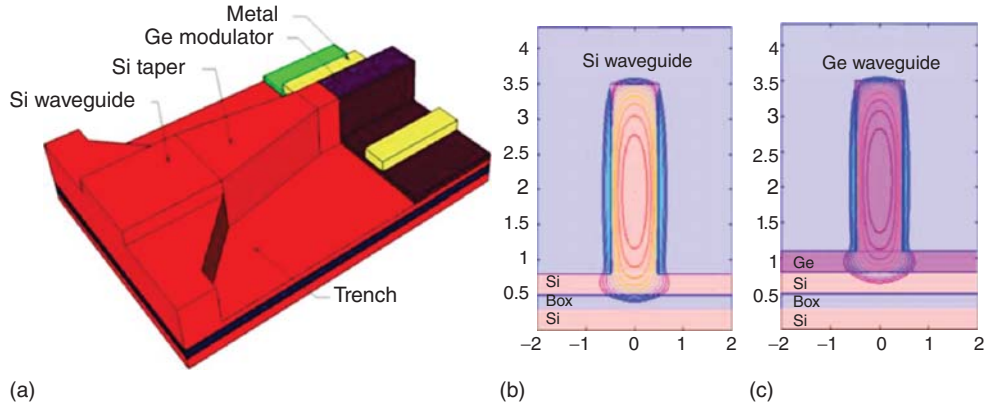

Figure 9.10 (a) Schematics of a tapered coupler for waveguide-coupling between a large core single mode Si ridge waveguide and the Ge EAM based on FKE. (b) Optical mode in the Si waveguide region before coupling. (c) Optical mode in the Ge EAM region. The theoretical coupling loss is 0.15 dB. Reproduced from Ref. [44] with permissions from OSA.

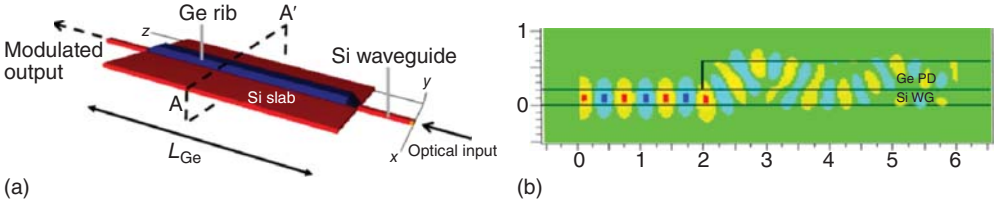

Figure 9.11 (a) Schematics of the evanescently coupled Ge EAM (based on FKE) reported by [50]. The Ge rib and the Si slab are 400 and 200 nm thick, respectively. Reproduced from Ref. [50] with the permissions of OSA. (b) FDTD simulation reported by Ref. [51] having the same thickness of the Ge and Si regions as (a). © 2010 IEEE. Reproduced, with permission, from Ref. [51].

EAMs if output coupling is also designed carefully to distribute the modulated light into different channels. The trade-off is that the Ge device area tends to be large.

Lim *et al.* [50] have reported evanescently coupled GeSi FKE modulators, as schematically shown in Figure 9.11a. The design falls into the "constant rate evanescent coupling regime" analyzed by Ahn *et al.* [51, 52]. In this case, the light oscillates between the Ge EAM active region and the Si slab underneath for optical modulation before it exits the output port of the waveguide. Because the thickness of Ge rib (400 nm) and Si slab (200 nm) are exactly the same as reported by Ahn *et al.* [51] in the theoretical analyses, the finite-difference time-domain (FDTD) simulation is shown in Figure 9.11b as a semi-quantitative indication of the oscillatory coupling between the Ge rib and the Si region underneath. Because the Ge region is still much thicker than Si, most of the optical power is confined in Ge, which enhances the efficiency of electroabsorption modulation. However,

an issue of the high confinement in Ge is that coupling to the output Si waveguide becomes difficult. Indeed, the insertion loss is >5 dB at $\lambda = 1620-1640$ nm even though the absorption of Ge in this wavelength regime is weak. At $\lambda = 1600$ nm the insertion loss increases to 9.6 dB.

9.4 Current Progress in Ge and GeSi EAMs

Table 9.1 summarizes the performance of Ge EAMs reported in recent years. Compared to Si MZI modulators based on free-carrier induced refractive index changes, GeSi EAMs are based on an ultrafast (<1 ps, [6]) and highly efficient field-induced change in absorption near the direct band edge, which enables a very compact device size and an ultralow capacitance. These features are especially advantageous for short-range applications such as photonic links in data centers. Compared to Si microring modulators, GeSi EAMs have a broader range of operation wavelengths and their performance is much less susceptible to temperature variations on chip.

The first waveguide-integrated GeSi EAM was demonstrated using tensile-strain enhanced FKE and a butt-coupling scheme [41]. The schematic device structure has been shown in Figure 9.9. Figure 9.12a shows a cross-sectional SEM photo of the device. The material was alloyed with 0.75% Si for operation at 1550 nm wavelength, according to the design in [7]. The active region consists of an n^+ Si/i–GeSi/p^+ Si vertical p–i–n diode structure. As the reserve bias is increased, the electric field in the GeSi region increases, leading to strong FKE that tilts the direct band edge toward longer wavelengths (Figure 9.12b).An extinction ratio of 8 dB at $\lambda = 1550$ nm was achieved with an insertion loss of 3.7 dB and a peak-to-peak voltage swing of $V_{pp} = 3$ V (from −4 to −7 V). The operational wavelength regime is 1539–1553 nm (Figure 9.12c), covering half of the C band. Owing to the compact size of the device ($0.6 \times 50\,\mu m^2$), the capacitance was as low as 11 fF. A conservative estimate of 50 fJ per bit energy consumption for 8 dB extinction ratio at $\lambda = 1550$ nm was reported based on $1/2\,CV_{pp}^2$, considering the most power-consuming scenario of flipping between "on" and "off" states in every operation. In digital communications, the average energy consumption would be $1/4\,CV_{pp}^2$ as the probability of flipping the bit in each operation is actually 50%. Under this consideration, the energy consumption would be as low as 25 fJ perbit (Figure 9.12d). A bandwidth of 1.2 GHz was demonstrated, mainly limited by the high series resistance due to fabrication error.

More recently, a 30 GHz waveguide-integrated Ge FKE modulator optimized for L-band (1610–1640 nm) operation [44] and a 40 GHz GeSi (0.7% Si) FKE modulator [47] optimized for 1550 nm operation have been demonstrated by Kotura, Inc. These devices utilized taper mode converters shown in Figure 9.10 for waveguide-coupling. An SEM image of a typical device structure is shown in Figure 9.13a. The extinction ratio and insertion loss spectra of the Ge EAM are shown in Figure 9.13b. The device demonstrated 2–5 dB insertion loss and

Table 9.1 Summary of Ge and GeSi EAM performance.

References	Optimal wave-length range (nm)	Coupling method	ER (dB)	IL (dB)	Band-width (GHz)	V_{pp} (V)	Active device area (μm²)	Average dynamic energy per bit $1/4CV_{pp}^2$ (fJ per bit)
Ge and GeSi FKE modulators								
[41]	1539–1553	Butt	8	3.7	1.2	3 (−4 to −7 V)	0.6 × 50	25[a]
[50]	1580–1610	Evanescent	10@1600 nm	9.6	1.25 Gb s^{-1}	5	0.8 × 20	10^2–10^3
[44]	1610–1640	Butt	6.3@1620 nm	3.6@1620 nm	30	4	1 × 45	~70
[47]	1545–1581	Butt	6	5	40.7	2.8	1 × 55	60
[53]	1525–1555	Butt	3	3	>40; >10 Gb s^{-1} for nine channels	2	–	50 for EAM; 570 including driver[b]
Ge QCSE modulators								
[54]	1441–1461	Side-entry	7.3@1457 nm	~9@1457 nm	–	10	450 × 450	–
[33]	1535–1545[c]	Side-entry	~6@1540 nm	–	–	4	225 × 625	–
[55]	1415–1440	Fiber coupled	7/10@1420 nm	3/7 dB@ 1420 nm	–	6	L = 34 or 64 μm	–
[56]	1425–1446	Fiber coupled	9@1435 nm V_{pp} = 1 V	15@1435 nm (−3 V)	23	1 (−3 to −4 V)	3 × 90	108
[48]	1450–1470 @-4 V DC bias[d]	Butt	>3.2@1460 nm	~15	3.5	1 (−3 to −5 V)	0.8 × 10	0.75
[37]	1290–1310	Fiber coupled	6@1293 nm	2.5	–	7	3 × 150	–

a) In [41] a conservative estimate of 50 fJ per bit was reported based on $1/2\,CV_{pp}^2$, considering the most power-consuming scenario of flipping between "on" and "off" states in every operation.
b) Integrated with 40 nm technology node CMOS driver and wavelength multiplexer.
c) Operating at 100 °C to reduce the direct band gap of the Ge QWs.
d) The operation wavelength range could be redshifted up to 1550 nm at a DC bias of −7.5 and 1 V voltage swing judging from the photocurrent measurement. The direct modulation data is only available at 1460 nm with −4 V DC bias, though.

The data are reported for 1550 nm operation, and the voltage swing is from 0 to $-V_{pp}$ (reverse bias) unless otherwise stated. ER refers to extinction ratio, and IL refers to insertion loss.
Adapted from Ref. [9].

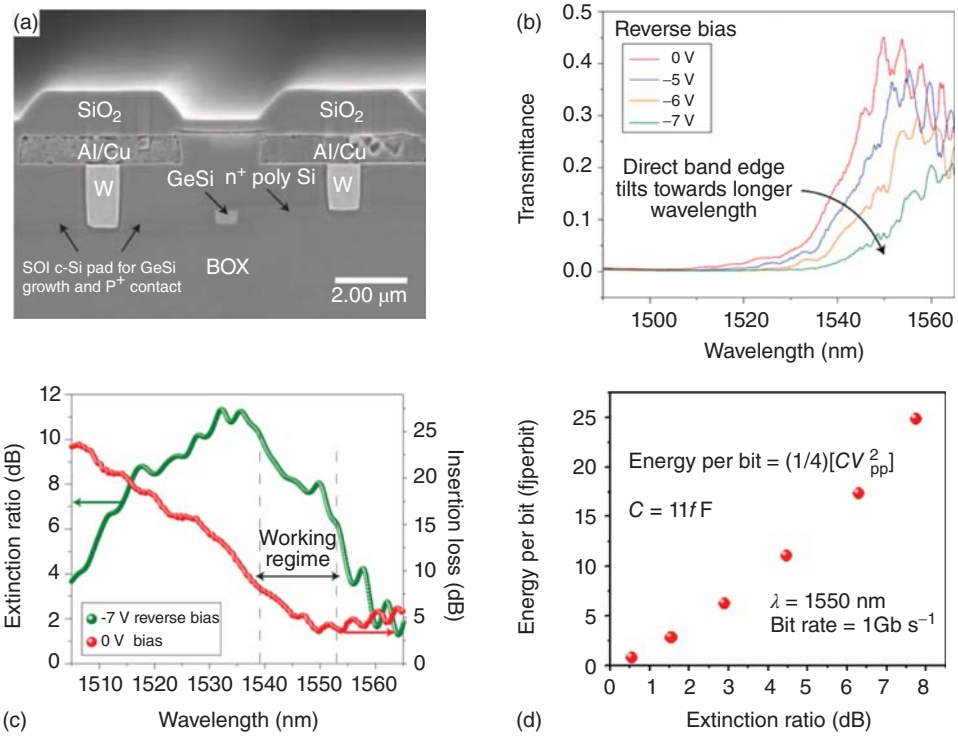

Figure 9.12 (a) Scanning electron microscopy photo showing a transverse cross-section of the first waveguide-integrated $Ge_{0.992}Si_{0.008}$ EAM [41]. The cross-section is taken perpendicular to the direction of light propagation. "W" refers to the W studs. "BOX" is buried oxide. (b) Transmittance spectra of the device under different reverse biases. (c) Insertion loss at 0 V bias and extinction ratio at −7 V reverse bias. The effective operation spectrum range is 1539–1553 nm. (d) Average dynamic energy consumption versus extinction ratio of the device. Reproduced from Ref. [41] under the Author's Copyright Agreement with Nature Publishing Group.

4–8 dB extinction ratio in the wavelength range of 1640–1610 nm. The $\Delta\alpha/\alpha$ reached 3.3 under 55 kV cm^{-1} electric field, which can be further improved by using narrower Ge intrinsic region so that a higher electric field can be achieved at the same reverse bias. To achieve C-band operation, 0.7 at% Si was incorporated into Ge. The insertion loss was 3–6 dB and extinction ratio 3–7 dB in the wavelength range of 1580–1540 nm (Figure 9.13c). The $\Delta\alpha/\alpha$ reached 3.1 under 75 kV cm^{-1} electric field. Figure 9.13d shows the frequency response of the device. A 3 dB frequency >20 GHz was achieved at a low voltage of 1 V. At 2.8 V reserve bias the 3 dB frequency exceeds 40 GHz.

Very lately, a nine-channel GeSi EAM array integrated with 40 nm technology node digital CMOS driver and wavelength multiplexer was reported, marking the entry of waveguide-coupled GeSi EAMs into system level integration [53]. Individual devices demonstrate a bandwidth >40 GHz. Figure 9.14a shows the

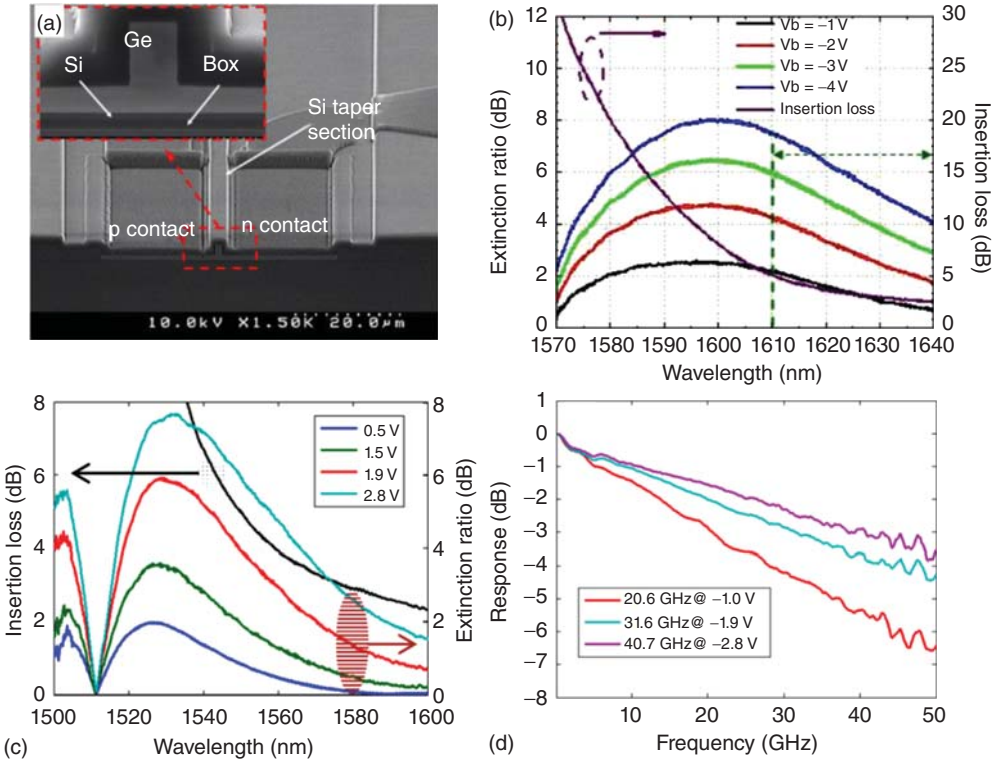

Figure 9.13 (a) SEM photo of a Ge EAM (based on FKE) reported by [44]. It corresponds to the device structure shown in Figure 9.10. (b) Insertion loss and extinction ratio spectra of the Ge EAM in (a). The operation wavelength range is 1610–1640 nm in the L band. (c) Insertion loss and extinction ratio spectra of a $Ge_{0.993}Si_{0.007}$ EAM (based on FKE) reported by [47]. With the addition of 0.7 at% Si the band edge is blueshifted for C-band operations around 1550 nm. (d) Frequency response of the device in (c), showing a 3 dB bandwidth exceeding 40 GHz. Reprinted from Refs. [44, 47] with permission from OSA.

transmission spectra of an unpackaged 10-channel device spaced at 100 GHz with an isolation >20 dB. Single channel operation upto 25 Gb s^{-1} and nine-channel operation at 10.25 Gb s^{-1} have been achieved at a low V_{pp} of 2 V (Figure 9.14b). The energy consumption of the EAM itself is as low as 50 fJ per bit, and the total energy is 570 fJ per bit including the modulator driver. Clearly, electrical rather than optical components are the major limiting factors of energy efficiency.

Lim *et al.* [57] have investigated GeSi ring modulators based on FKE-induced refractive index changes. As discussed in Section 9.2.1 and Figure 9.2, FKE can also induce a significant change in the real part of refract index (Δn) with a high EO coefficient. However, a significant challenge for device application is the losses from the indirect gap absorption. Lim *et al.* [57] first reported a $Ge_{0.97}Si_{0.03}$ race track ring modulator with a refractive index change of 2.6×10^{-5} under an applied

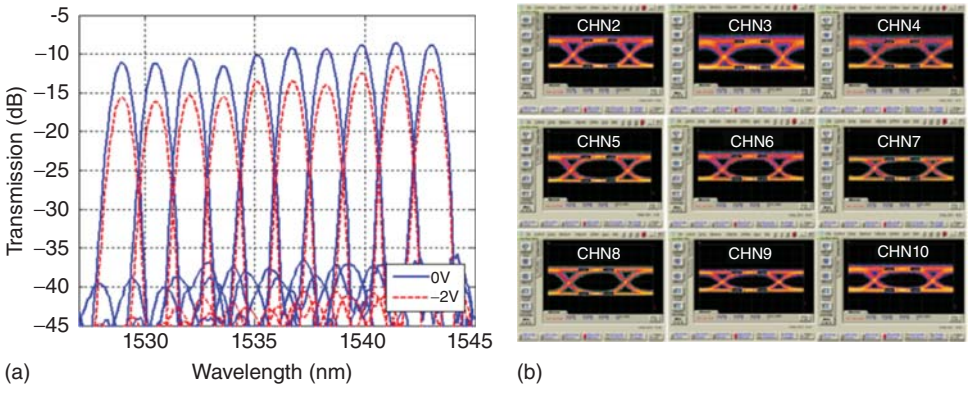

Figure 9.14 (a) Transmission spectra of an unpackaged 10-channel GeSi FKE modulator + multiplexer array chip reported by [53]. (b) Eye diagrams at 10.25 Gb s^{-1} for a packaged nine-channel device chip. Center wavelength is 1532 nm and separation between channels is 1.6 nm.

field of ~45 kV cm^{-1}. The electric field is estimated from the reported 7 V reverse bias applied over an electrode-to-electrode distance of 1.5 μm. The 2.9% Si composition was chosen to reduce the indirect gap absorption in the C-band while still maintaining a reasonable EO coefficient. To improve the ring modulator performance, Lim *et al.* [58] further proposed a coupled Si outer ring/GeSi inner-ring EAM structure, as shown in Figure 9.15a.The outer ring is essentially a regular add-drop ring filter. Unlike concentric ring resonators, the thin single mode GeSi inner ring is intentionally non-guiding, and the loss is tunable by FKE to achieve modulation. Therefore, it does not require the precise alignment of multiple inner ring/outer ring modes. In addition to tuning the Si composition, the gap between the inner GeSi ring and outer Si ring provides another handle to modify the coupling and optimize the device performance. As shown in Figure 9.15b, with 3 V reverse bias applied on a 150 nm-thick $Ge_{0.995}Si_{0.005}$ inner ring and a gap of 100 nm between the inner and outer rings, extinction ratios of 6.5 and 5.0 dB can be achieved at $\lambda = 1547.6$ nm for the through and drop ports, respectively. The corresponding insertion losses are 4.4 and 2.9 dB, respectively.

The first Ge QCSE modulator was demonstrated using a side-entry approach [54]. The light was coupled through the edge of a lightly doped Si wafer, then incident on a Ge QW mesa grown on top of it. A 7.3 dB extinction ratio at 1457 nm was demonstrated with a V_{pp} of 10 V. Improving upon this work, Roth *et al.* [33] further demonstrated a Ge QCSE modulator working in C-band by heating up the sample to 100 °C in order to reduce the direct band gap of the Ge QW. The transmittance spectra of this device have been shown in Figure 9.6a. An extinction ratio of 3 dB was achieved at 1539–1543 nm using a low V_{pp} of 1 V between −3.6 and −4.6 V reserve bias. For $V_{pp} = 4$ V, the extinction ratio is increased to >6 dB at 1536–1545 nm.

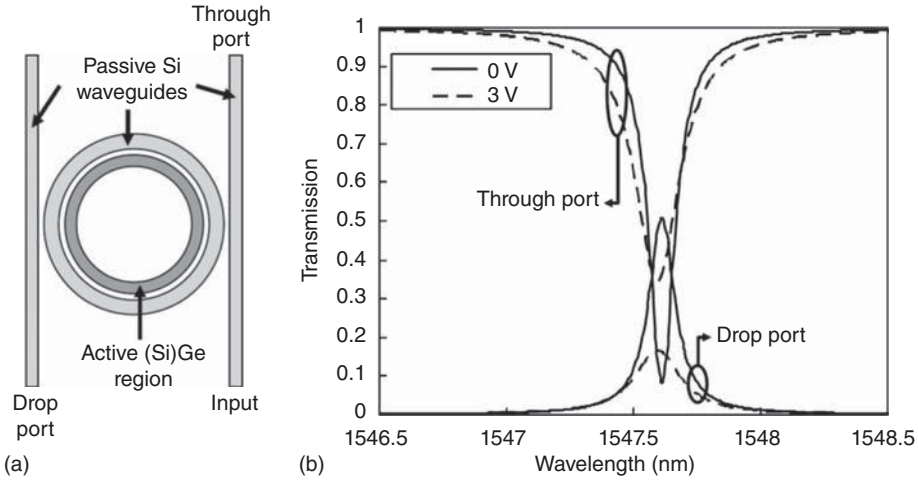

Figure 9.15 (a) The GeSi ring EAM structure proposed by [58]. (b) Modeled transmission spectra at the through port and the drop port under 0 and 3 V reverse bias. The thickness of the $Ge_{0.995}Si_{0.005}$ layer is 150 nm. Reprinted from Ref. [58] with permissions from OSA.

Ge QCSE modulators directly coupled to taper-lensed fibers were investigated by Chaisakul *et al.* [55]. An extinction ratio greater than 7 dB has been demonstrated at ~1420 nm with ~3 dB insertion loss for a 34 μm-long device. The same group later achieved 23 GHz modulators with 9 dB extinction ratio and $V_{pp} = 1$ V (between −3 and −4 V reverse bias) [56], as shown in Figure 9.16a. The insertion loss is partially due to the indirect gap absorption in the thick $Si_{0.1}Ge_{0.9}$ buffer layer, as indicated by the mode profile in Figure 9.16b. It could be reduced by using a thinner buffer layer. As discussed earlier in Section 9.2.2, the same group has also demonstrated a Ge QCSE modulator with $Si_{0.35}Ge_{0.65}$ barrier layers working at 1300 nm very recently (Figure 9.7, [37]), covering another important wavelength in optical communications.

The first waveguide-integrated Ge QCSE modulator was demonstrated on an SOI substrate using a butt-coupling approach (Figure 9.17a, [48]). From the photocurrent ratio measurement (Figure 9.17b) under different reserve biases, it was suggested that a 3 dB extinction ratio could be achieved using 1 V swing. With the increase of DC reverse bias the response can also be extended to longer wavelengths. A 3.5 GHz bandwidth was demonstrated at 1460 nm with an extinction ratio >3 dB, using an impressively compact device of $0.8 \times 10\,\mu m^2$ (Figures 9.17c). Although the insertion loss is large due to the optical modal mismatch between the SOI waveguide and the Ge QW active region, it could be improved by optimizing the device design and fabrication. The ultralow capacitance of the device (0.75 fF) and low $V_{pp} = 1$ V are highly advantageous for energy-efficient modulation on the order of 1 fJ per bit. It is expected that the required DC voltage offset could also be reduced using the improved QW design in [34].

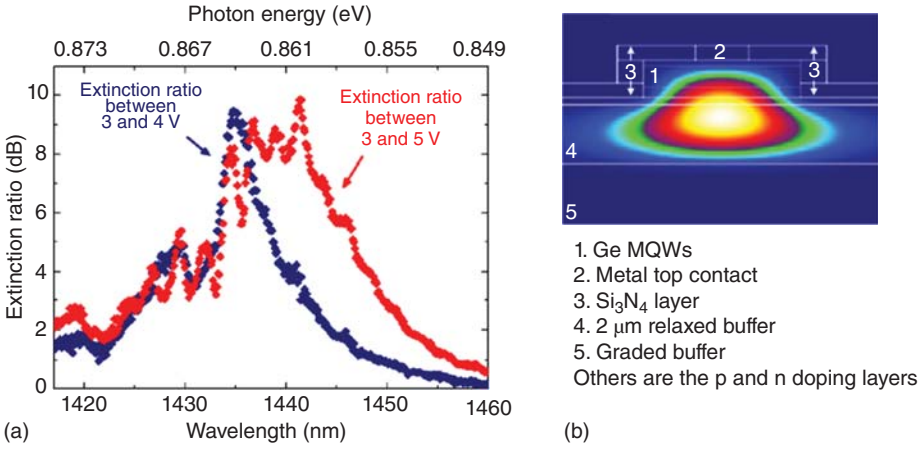

Figure 9.16 (a) Extinction spectra at $V_{pp} = 1\,V\,(3–4\,V)$ and $V_{pp} = 2\,V\,(3–5\,V)$ for the Ge QCSE modulator reported by [56]. (b) The corresponding mode profile in the device. A large fraction of the optical mode is in the SiGe buffer layer, which increases the insertion loss.

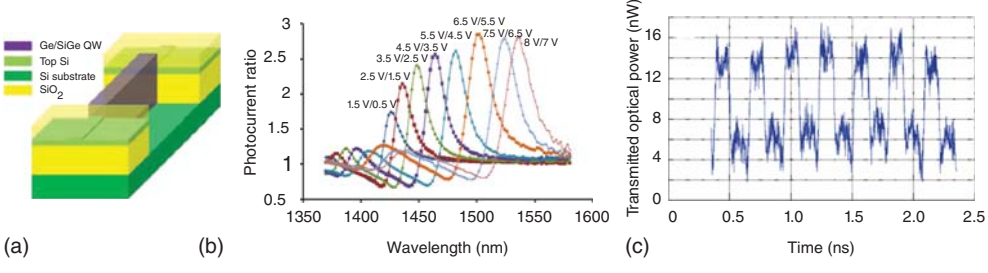

Figure 9.17 (a) Schematic device structure of the waveguide-integrated Ge QCSE modulator reported by [48]. (b) The photocurrent ratio of the device with 1 V swing under different DC reserve bias offsets. (c) The modulated signals at 3.5 GHz. © 2012 IEEE Reprinted, with permissions, from Ref. [48].

9.5 Conclusions

In this chapter we have discussed the working principles, waveguide- coupling, and the latest progress in Ge and GeSi EAMs based on FKE and QCSE. The waveguide-integrated Ge and GeSi FKE modulators have achieved a bandwidth greater than 40 GHz, a low energy consumption ≤50 fJ per bit, and a reasonably broad operation wavelength range for multi-channel wavelength division multiplexing (WDM) applications. They can very well cover the S, C, L bands in optical communications. Owing to their simplicity in fabrication and device integration, Ge and GeSi EAMs based on FKE have entered system level applications, and they are being commercialized by industries. Ge EAMs based on QCSE have demonstrated great potential in achieving ultralow energy operation on the order

of 1 fJ per bit in both 1310 and 1550 nm communication wavelength windows. The results in Table 9.1 indicate that Ge and GeSi EAMs are ideal candidates for high bandwidth, high energy-efficiency photonic modulators monolithically integrated on Si.

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10
Strained Ge for Si-Based Integrated Photonics

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10.1
Introduction

Integration of photonics with electronics is a current thrust to meet the ever-increasing demand on the bandwidth of computing and communication. This is because photonics is capable of a bandwidth increase by a couple of orders using wavelength division multiplexing (WDM) and advanced modulation formats such as phase space keying. The bandwidth density should be substantially increased with electronics and photonics integration on a Si complementary metal oxide semiconductor (CMOS) platform. The challenging issue is the presence of a large variety of devices and materials in photonics: In electronics, there are basically two devices: transistor and electric interconnect and these devices consists of Si, O, N, Al, that is, the most abundant materials on the earth and are primarily being used with the Si CMOS platform. That is referred to as CMOS-compatible materials. In contrast, photonics need light emitter, optical modulator, multiplexor/demultiplexor, photodetector, isolator, optical interconnect, and so on. This large diversity of devices ends up with a wide variety of materials sets such as III–Vs light emitter and photodetector, $LiNbO_3$ modulator, SiO_2 optical interconnect, Fe Garnet based isolator, and so on. These diversities in materials and devices would be a red brick of photonics integration with electronics on the Si CMOS platform. There are two ways to break through this challenging issue in photonics integration: jumping up one rank higher algorism hierarchy from the current Neumann Architecture and reducing materials or devices diversities themselves. Binary decision diagram algorism has been known as an excellent way to jump up and has recently demonstrated the function based on Si photonics [1]. To stay in the current architecture, CMOS compatible material set should be used to realize such photonic functions on a chip. Ge should be the key material for this, as it works as emitter [2, 3], modulator [4], and detector [5]. On Si and it is known as the CMOS compatible material as in Chapter 6 in this book. The rest of the devices besides an isolator are now all based on Si. This chapter explains that Ge is an enabler in electronics and photonics convergence.

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WDM in fiber optics utilizes various wavelength channels to transmit signals and uses 1530–1625 nm to cover C + L bands. Thus, to implement WDM in Si photonics, the photodetector, modulator, and light emitter should be capable of working at the wavelength range. These device functions are basically governed by the Ge direct bandgap (−0.8 eV = 1550 nm). Therefore, it would be appropriate to tune the Ge bandgap, which can be done by strain engineering of the bandgap.

10.2 Bandgap and Strain: Theory

Ge and Si are semiconductors of the diamond structure, and GaAs described later is of zincblende structure. The strain of these materials can be generalized as follows [6]. Here, we should assume a small deformation of elastic solid. The Hooke's law can predict the linear relation between stress tensor σ_{ij} and strain tensor ε_{kl}, that is,

$$\sigma_{ij} = c_{ijkl}\varepsilon_{kl}, \tag{10.1}$$

where $c_{ij\,kl}$ is the elastic stiffness tensor. Under the cubic symmetry c can be expressed only by three coefficients, c11, c12, and c44. Thus, Eq. (10.1) can be simplified and inversely expressed by the following equations with elastic compliance tensor s_{ij}:

$$\begin{pmatrix}\sigma_{11}\\ \sigma_{22}\\ \sigma_{33}\\ \sigma_{23}\\ \sigma_{31}\\ \sigma_{12}\end{pmatrix} = \begin{pmatrix} c_{11} & c_{12} & c_{12} & 0 & 0 & 0\\ c_{12} & c_{11} & c_{12} & 0 & 0 & 0\\ c_{12} & c_{12} & c_{11} & 0 & 0 & 0\\ 0 & 0 & 0 & c_{44} & 0 & 0\\ 0 & 0 & 0 & 0 & c_{44} & 0\\ 0 & 0 & 0 & 0 & 0 & c_{44}\end{pmatrix}\begin{pmatrix}\varepsilon_{11}\\ \varepsilon_{22}\\ \varepsilon_{33}\\ 2\varepsilon_{23}\\ 2\varepsilon_{31}\\ 2\varepsilon_{12}\end{pmatrix}, \tag{10.2}$$

$$\begin{pmatrix}\varepsilon_{11}\\ \varepsilon_{22}\\ \varepsilon_{33}\\ 2\varepsilon_{23}\\ 2\varepsilon_{31}\\ 2\varepsilon_{12}\end{pmatrix} = \begin{pmatrix} s_{11} & s_{12} & s_{12} & 0 & 0 & 0\\ s_{12} & s_{11} & s_{12} & 0 & 0 & 0\\ s_{12} & s_{12} & s_{11} & 0 & 0 & 0\\ 0 & 0 & 0 & s_{44} & 0 & 0\\ 0 & 0 & 0 & 0 & s_{44} & 0\\ 0 & 0 & 0 & 0 & 0 & s_{44}\end{pmatrix}\begin{pmatrix}\sigma_{11}\\ \sigma_{22}\\ \sigma_{33}\\ \sigma_{23}\\ \sigma_{31}\\ \sigma_{12}\end{pmatrix}. \tag{10.3}$$

Here, elastic compliance is expressed using elastic stiffness as follows:

$$s_{11} = \frac{c_{11} + c_{12}}{(c_{11} - c_{12})(c_{11} + 2c_{12})}, \tag{10.4}$$

$$s_{12} = \frac{-c_{12}}{(c_{11} - c_{12})(c_{11} + 2c_{12})}, \tag{10.5}$$

$$s_{44} = \frac{1}{c_{44}}. \tag{10.6}$$

Table 10.1 shows elastic stiffness constants of Ge, Si, and GaAs.

Table 10.1 Elastic stiffness constants of Ge, Si, and GaAs.

		c (GPa)		*s* (/GPa)
GaAs	c_{11}	118.8	s_{11}	1.17×10^{-2}
	c_{12}	53.8	s_{12}	-3.65×10^{-3}
	c_{44}	59.4	s_{44}	1.68×10^{-2}
Si	c_{11}	165.8	s_{11}	7.68×10^{-3}
	c_{12}	63.9	s_{12}	-2.14×10^{-3}
	c_{44}	79.6	s_{44}	1.26×10^{-2}
Ge	c_{11}	128.5	s_{11}	9.80×10^{-3}
	c_{12}	48.3	s_{12}	-2.68×10^{-3}
	c_{44}	66.8	s_{44}	1.50×10^{-2}

Equation (10.3) will give specific strain versus amount of stress along specific directions. Let us consider stress σ applied to a crystals along [100] direction. Here, we assume that stresses along other directions are 0.

$$\begin{pmatrix} \varepsilon_{xx} \\ \varepsilon_{yy} \\ \varepsilon_{zz} \\ 2\varepsilon_{yz} \\ 2\varepsilon_{zx} \\ 2\varepsilon_{xy} \end{pmatrix} = \begin{pmatrix} s_{11} \\ s_{12} \\ s_{12} \\ 0 \\ 0 \\ 0 \end{pmatrix} \sigma. \tag{10.7}$$

Let us consider the case in which stress is applied along the [110] direction. Here, we define x as [100], y as [010], and z as [001], and then [110] as x', [1−10] as y', and [001] as z'. With $x'y'z'$ coordinate, stress can be written by:

$$\begin{pmatrix} \sigma_{x'x'} & \sigma_{x'y'} & \sigma_{x'z'} \\ \sigma_{y'x'} & \sigma_{y'y'} & \sigma_{y'z'} \\ \sigma_{z'x'} & \sigma_{z'y'} & \sigma_{z'z'} \end{pmatrix} = \begin{pmatrix} \sigma & 0 & 0 \\ 0 & 0 & 0 \\ 0 & 0 & 0 \end{pmatrix}. \tag{10.8}$$

To transform Eq. (10.8) to xyz coordinate, we can use rotation matrix $U(\theta)$ to rotate −45°. In other words, we have

$$\begin{pmatrix} \sigma_{xx} & \sigma_{xy} & \sigma_{xz} \\ \sigma_{yx} & \sigma_{yy} & \sigma_{yz} \\ \sigma_{zx} & \sigma_{zy} & \sigma_{zz} \end{pmatrix} = U(\theta) \begin{pmatrix} \sigma_{x'x'} & \sigma_{x'y'} & \sigma_{x'z'} \\ \sigma_{y'x'} & \sigma_{y'y'} & \sigma_{y'z'} \\ \sigma_{z'x'} & \sigma_{z'y'} & \sigma_{z'z'} \end{pmatrix} U^T(\theta), \tag{10.9}$$

$$U(\theta) = \begin{pmatrix} \cos\theta & \sin\theta & 0 \\ -\sin\theta & \cos\theta & 0 \\ 0 & 0 & 1 \end{pmatrix}. \tag{10.10}$$

By plugging Eqs (10.8) and (10.10) into Eq. (10.9), and $\theta = -45°$, we get

$$\begin{pmatrix} \sigma_{xx} & \sigma_{xy} & \sigma_{xz} \\ \sigma_{yx} & \sigma_{yy} & \sigma_{yz} \\ \sigma_{zx} & \sigma_{zy} & \sigma_{zz} \end{pmatrix} = \frac{\sigma}{2} \begin{pmatrix} 1 & 1 & 0 \\ 1 & 1 & 0 \\ 0 & 0 & 0 \end{pmatrix}. \tag{10.11}$$

Equations (10.3) and (10.11) give us:

$$\begin{pmatrix} \varepsilon_{xx} \\ \varepsilon_{yy} \\ \varepsilon_{zz} \\ 2\varepsilon_{yz} \\ 2\varepsilon_{zx} \\ 2\varepsilon_{xy} \end{pmatrix} = \begin{pmatrix} \frac{s_{11}+s_{12}}{2} \\ \frac{s_{11}+s_{12}}{2} \\ s_{12} \\ 0 \\ 0 \\ \frac{s_{44}}{2} \end{pmatrix} \sigma. \tag{10.12}$$

Now, we use the deformation potential method to understand the effects of hydrostatic train component on bandgap. The modulation of valence bands by strain is expressed by

$$\Delta E_{v,av} = a_v(\varepsilon_{xx} + \varepsilon_{yy} + \varepsilon_{zz}), \tag{10.13}$$

where a_v denotes hydrostatic deformation potential. Similarly the modulation of conduction bands is

$$\Delta E_{c,av} = a_c(\varepsilon_{xx} + \varepsilon_{yy} + \varepsilon_{zz}). \tag{10.14}$$

Finally, spin–orbit interaction splits heavy hole band and light hole band and one of which determines the valence band top, which is given by

$$E_{v,\text{top}} = E^0_{v,av} + \frac{\Delta_0}{3}, \tag{10.15}$$

where $E_{v,\text{top}}$ is valence band with no strain, Δ_0 spin orbit splitting energy. The conduction band bottom is also expressed by

$$E_{c,\text{btm}} = E_{v,\text{top}} + E_g. \tag{10.16}$$

Based on these derivations, we can derive the effect of bandgap modulation by [100] stress applied to a crystal where strain is the hydrostatic component. First the valence band can be expressed by

$$\Delta E_{v,HH} = \frac{1}{3}\Delta_0 - \frac{1}{2}\delta E_{100}, \tag{10.17}$$

$$\Delta E_{v,LH} = -\frac{1}{6}\Delta_0 + \frac{1}{4}\delta E_{100} + \frac{1}{2}\left[{\Delta_0}^2 + \Delta_0\delta E_{100} + \frac{9}{4}\left(\delta E_{100}\right)^2\right]^{1/2}, \tag{10.18}$$

$$\Delta E_{v,SO} = -\frac{1}{6}\Delta_0 + \frac{1}{4}\delta E_{100} - \frac{1}{2}\left[\Delta_0^2 + \Delta_0\delta E_{100} + \frac{9}{4}\left(\delta E_{100}\right)^2\right]^{1/2}, \tag{10.19}$$

where δE_{100} is the sheer strain deformation potential, and is given by

$$\delta E_{100} = 2b(\varepsilon_{xx} - \varepsilon_{zz}). \tag{10.20}$$

No band splitting occurs in conduction bands because the crystal symmetry is preserved under strain.

[110] stress similarly modulates the valence band as expressed:

$$\begin{pmatrix} \frac{\Delta_0}{3} - \frac{1}{8}\left(\delta E_{001} + 3\delta E_{111}\right) & -\frac{\sqrt{3}}{8}(\delta E_{001} - \delta E_{111}) & \frac{\sqrt{6}}{8}(\delta E_{001} - \delta E_{111}) \\ -\frac{\sqrt{3}}{8}(\delta E_{001} - \delta E_{111}) & \frac{\Delta_0}{3} + \frac{1}{8}(\delta E_{001} + 3\delta E_{111}) & \frac{\sqrt{2}}{8}(\delta E_{001} + 3\delta E_{111}) \\ \frac{\sqrt{6}}{8}(\delta E_{001} - \delta E_{111}) & \frac{\sqrt{2}}{8}(\delta E_{001} + 3\delta E_{111}) & -\frac{2}{3}\Delta_0 \end{pmatrix}, \tag{10.21}$$

where δE_{100} and δE_{111} can be given by:

$$\delta E_{001} = 4b(\varepsilon_{xx} - \varepsilon_{zz}), \tag{10.22}$$

$$\delta E_{111} = \frac{4}{\sqrt{3}} d\varepsilon_{xy}, \tag{10.23}$$

where d is the sheer component deformation potential.

L valley of conduction band can be expressed with

$$\Delta E_c^{111,11\bar{1}} = \frac{2}{3}\Xi_u^L \varepsilon_{xy}, \tag{10.24}$$

$$\Delta E_c^{\bar{1}11,1\bar{1}1} = -\frac{2}{3}\Xi_u^L \varepsilon_{xy}. \tag{10.25}$$

Using the above equations, the valence and conduction bands under strain [100] are expressed to be

$$E_v^{HH} = \{a_v(s_{11} + 2s_{12}) - b(s_{11} - s_{12})\}\sigma, \tag{10.26}$$

$$E_v^{LH} = \left\{ a_v\left(s_{11} + 2s_{12}\right) + \frac{b}{2}(s_{11} - s_{12}) \right\}\sigma - \frac{1}{2}\Delta_0 + \frac{1}{2}\sqrt{9b^2(s_{11} - s_{12})^2\sigma^2 + 2b\Delta_0(s_{11} - s_{12})\sigma + {\Delta_0}^2}, \tag{10.27}$$

$$E_v^{LH} = \left\{ a_v\left(s_{11} + 2s_{12}\right) + \frac{b}{2}(s_{11} - s_{12}) \right\}\sigma - \frac{1}{2}\Delta_0 - \frac{1}{2}\sqrt{9b^2(s_{11} - s_{12})^2\sigma^2 + 2b\Delta_0(s_{11} - s_{12})\sigma + {\Delta_0}^2}, \tag{10.28}$$

$$E_c^{\Gamma} = a_c^{\Gamma}(s_{11} + s_{12})\sigma + E_g^{\Gamma}, \tag{10.29}$$

$$E_c^{L} = a_c^{L}(s_{11} + s_{12})\sigma + E_g^{L}. \tag{10.30}$$

However, the valence band under strain [110] can only be expressed by eigen value of the following determinant:

$$\begin{pmatrix} -\frac{1}{8}\left\{2b\left(s_{11}-s_{12}\right)+\sqrt{3}ds_{44}\right\}\sigma & -\frac{1}{8}\{2\sqrt{3}b(s_{11}-s_{12})-ds_{44}\}\sigma & \frac{1}{8}\{2\sqrt{6}b(s_{11}-s_{12})-\sqrt{2}ds_{44}\}\sigma \\ -\frac{1}{8}\{2\sqrt{3}b(s_{11}-s_{12})-ds_{44}\}\sigma & \frac{1}{8}\{2b(s_{11}-s_{12})+\sqrt{3}ds_{44}\}\sigma & \frac{1}{8}\{2\sqrt{2}b(s_{11}-s_{12})+\sqrt{6}ds_{44}\}\sigma \\ \frac{1}{8}\{2\sqrt{6}b(s_{11}-s_{12})-\sqrt{2}ds_{44}\}\sigma & \frac{1}{8}\{2\sqrt{2}b(s_{11}-s_{12})+\sqrt{6}ds_{44}\}\sigma & -\Delta_0 \end{pmatrix}. \tag{10.31}$$

Then the conduction band can be written by

$$E_c^{\Gamma} = a_c^{\Gamma}(s_{11}+2s_{12})\sigma + E_g^{\Gamma}, \tag{10.32}$$

$$E_c^{L}(111,11\bar{1}) = \left\{a_c^{L}\left(s_{11}+2s_{12}\right)+\frac{1}{6}\Xi_u^{L}s_{44}\right\}\sigma + E_g^{L} \tag{10.33}$$

$$E_c^{L}(\bar{1}11,1\bar{1}1) = \left\{a_c^{L}\left(s_{11}+2s_{12}\right)-\frac{1}{6}\Xi_u^{L}s_{44}\right\}\sigma + E_g^{L} \tag{10.34}$$

Based on these formulations, we can calculate the strain versus bandgap of Si, Ge, and GaAs as discussed in the next section.

10.3 Bandgap and Strain: Experiment

10.3.1 Si

The bandgap versus strain in one dimension and two dimensions calculated are summarized in Figure 10.1 [7]. Here, we have first used Si as a typical example. This indicates that tensile strain and compressive strain shrink the bandgap. One dimensional strain alters the bandgap less effectively than two dimensional strain, as can be intuitively understood.

To strain semiconductors, we have chosen a cantilever structure, that is, beam in this chapter as in Figure 10.2. The simulation shows non-uniform strain distribution in this Si beam structure. Here, the beam is vertically pushed down at the tip of the beam as in Figure 10.3. It is clearly understood that the

1) strain on the top of the beam is tensile while on the bottom it is compressive.
2) strain is the highest at the beam edge while it is the smallest at the beam tip (near the point pushed in Figure 10.3).

This, together with Figure 10.1, indicates that the bandgap can be locally controlled by the strain in the beam structure.

To demonstrate the strain effect on Si bandgap, we made the Si beam structure using silicon on insulator (SOI) wafers [8]. The vertical structure of SOI is a 200 nm thick Si film on a 3 μm thick SiO_2 layer on a Si wafer. By opening the top Si film through dry etching in a shape like the letter U as in Figure 10.3, and then dipping it into hydrofluoric acid to remove SiO_2, we can get the Si beam structure. Scanning electron microscopy (SEM) reveals the Si beam structure as

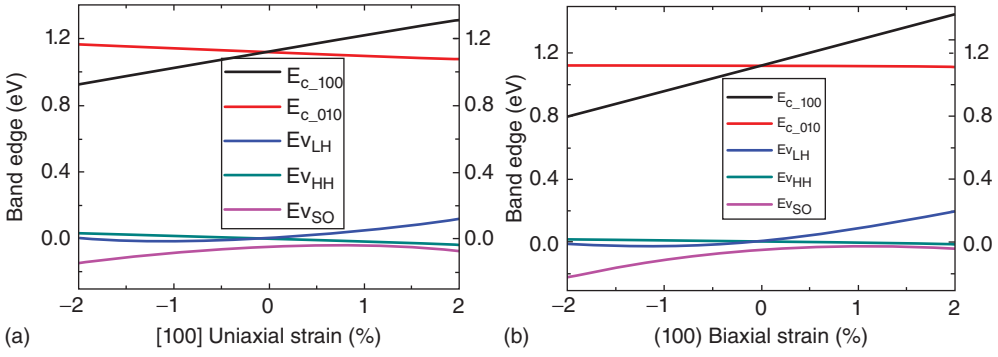

Figure 10.1 Strain versus bandgap of Si. (a) [100] uniaxial strain, (b) biaxial strain on (100).

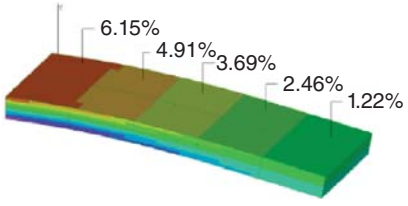

Figure 10.2 Simulation of strain distribution in Si cantilever structure with external force at its tip.

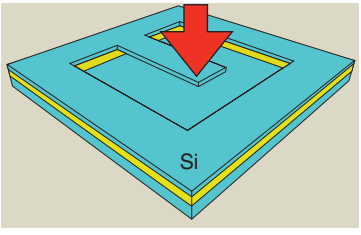

Figure 10.3 Schematics of Si beam fabricated using SOI wafer. Blue: Si and yellow: SiO_2.

in Figure 10.4. The beam allows us to change the strain by pushing down the beam at various points such as Bent 3, 2, and 1 in Figure 10.4. We have used microscopic photoluminescence (μ-PL) spectroscopy to get its bandgap versus strain relationships. The excitation laser 457 nm was focused on the beam edge shown by "X" in Figure 10.4 to locally measure the photoluminescence (PL) spectra with various strains. Typical spectra are shown in Figure 10.5 [8]. It is clearly shown from Figure 10.5 that there are two types of peaks in these PL spectra: one is a broad in wavelength and the other is sharp. The former is due to electron-hole recombination across the bandgap of Si, and the latter is due to resonances of PL light, that is, Fabry–Perot fringes [9]. It was found from the resonance wavelength spacings that the Fabry–Perot resonator is formed by the two sidewalls of the beam. Figure 10.5 indicates that:

1) the bandgap is located at ~1100 nm without strain (Straight), as expected from the Si bandgap,

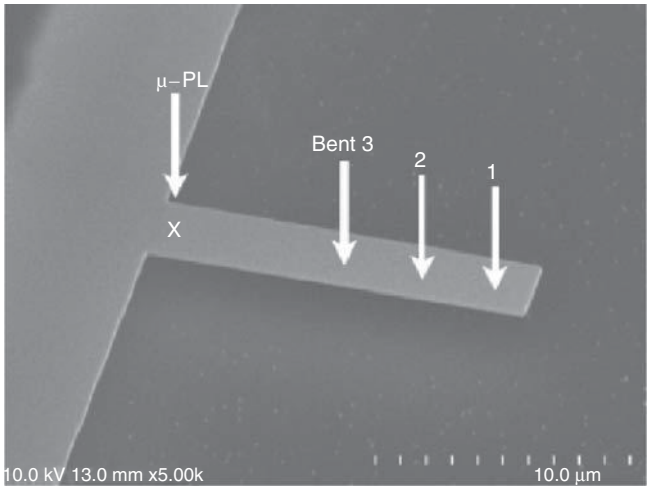

Figure 10.4 SEM image of Si beam. The points named "Bent 1–3" are to stress externally.

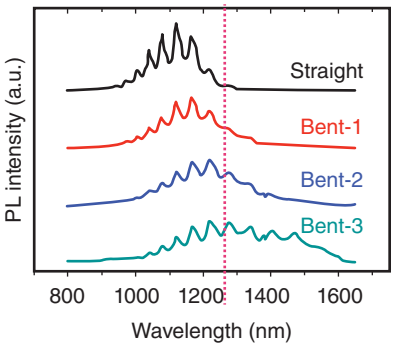

Figure 10.5 Photoluminescence spectra measured at *x* in Figure 10.4. Stress shrinks the bandgap of Si.

2) when we stressed the beam at the point (Bent 1), the PL peak shows red-shift, and the red-shift increases with increase in strain, that is, the pushing point becomes closer to the beam edge (Bent 2 and 3).
3) Bent 3 shifted the PL peak located beyond 1400 nm.

These observations were well reproduced by theoretical calculations. This proves our concept of bandgap tuning by strain.

We have shown only the imaginary part of the complex refractive index in this chapter. However, we have reported that evenstronger strain altered the real part of the complex refractive index in terms of the Kromars–Kronig relation [7].

10.3.2 Ge on Si

Ge on Si beam can be fabricated using the process described in the Si beam section above. The difference is only the starting material. Here, we used a Ge epilayer on

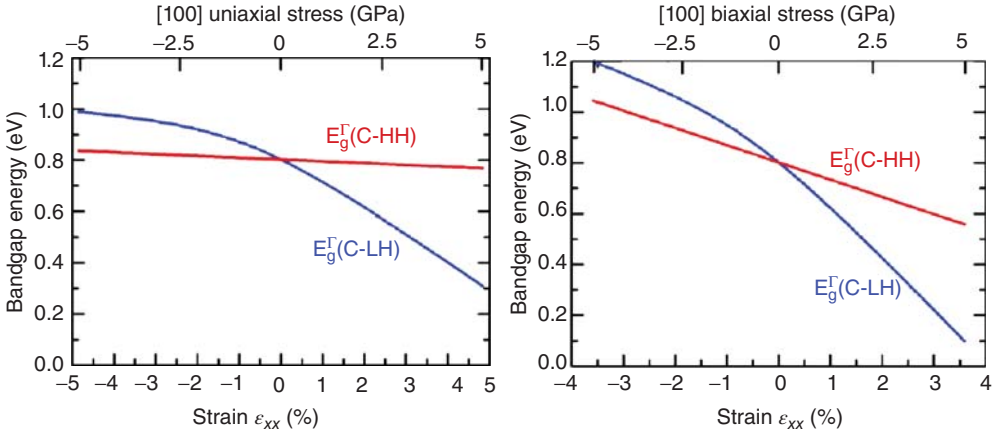
[100] uniaxial stress (GPa)
−5 −2.5 0 2.5 5
Bandgap energy (eV)
1.2 1.0 0.8 0.6 0.4 0.2 0.0
E_g^{Γ}(C-HH)
E_g^{Γ}(C-LH)
−5 −4 −3 −2 −1 0 1 2 3 4 5
Strain ε_{xx} (%)
[100] biaxial stress (GPa)
−5 −2.5 0 2.5 5
Bandgap energy (eV)
1.2 1.0 0.8 0.6 0.4 0.2 0.0
E_g^{Γ}(C-HH)
E_g^{Γ}(C-LH)
−4 −3 −2 −1 0 1 2 3 4
Strain ε_{xx} (%)

Figure 10.6 Strain versus bandgap of Ge.

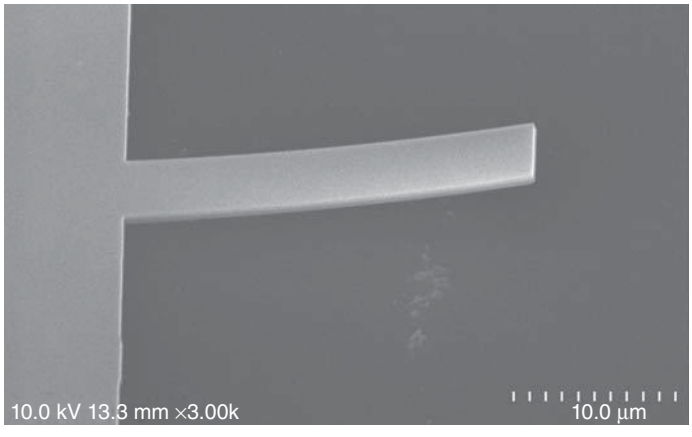

Figure 10.7 SEM image of Ge on Si beam.

SOI instead of SOI. The bandgap expansion and shrinkage are basically similar as in the case of Si. Here, Figure 10.6 shows uniaxial and biaxial strain dependence on the bandgap of Ge. The one dimensional strain along [110] was similar to the [100] directions.

Figure 10.7 shows an SEM image of fabricated Ge on Si beam. It should be noted that the Ge on Si beam shows upbending about 2 µm from horizon. The upbending should occur by the thermal mismatch of the linear expansion coefficients of Si and Ge. As noted above, Ge has a built-in tensile strain about 0.1–0.2%, leading to this upbending. Theoretical calculation reproduced the amount of upbending.

The vertical force was applied to the tip of the Ge on Si beam. The location is shown as Bend 1 in Figure 10.4 and µPL was measured at the point X. Figure 10.8

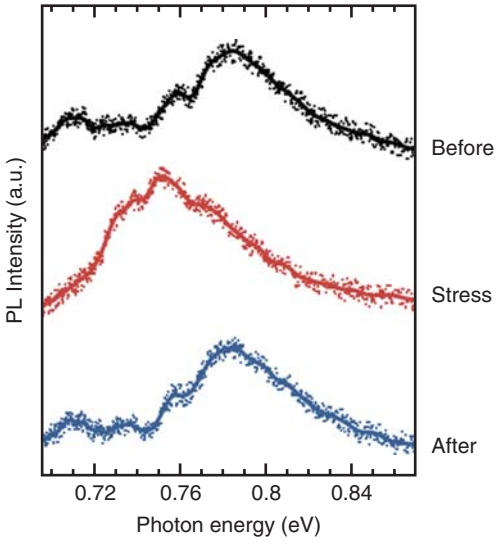

Figure 10.8 Photoluminescence spectra with and without stressing. Black: before stressing, red: under stressing, and blue: after stressing.

shows PL spectra from the Ge on Si beam. Before bending, the PL peak is located at ~0.8 eV because the beam is relaxed and the built-in tensile strain is almost zero. Under the external force to push down the beam, the peak is at ~0.76 eV. The red-shift amount 35 meV corresponded to the strain 0.56% from Figure 10.6. This is the exact amount of strain introduced by the beam bending. After releasing the external force, the PL spectrum restores the original peak, which indicates that the red-shift of the spectrum is due to the elastic strain and not due to deformation-induced defects.

10.3.3 GaAs on Ge on Si

It is well known that Ge has an almost identical lattice constant to GaAs. Thus, GaAs can be epitaxially grown on Ge. The off-cut Ge is necessary to avoid antiphase domain boundaries. Here, we have grown a GaAs epi on Ge on off-cut SOI wafers. Here, the off-cut was 6° along <110> directions. Figure 10.9 shows the strain versus bandgap relation of GaAs [10].

Figure 10.10 shows the TEM image of the GaAs on Ge on an SOI layer. It is clearly shown that there is no dislocations at the GaAs and Ge interface, while there are many dislocations at the Ge and Si interface. This can be understood considering the lattice mismatch among the layer structure. It is worth mentioning that the GaAs on the Ge on Si beam showed upbending as it appeared in the Ge on Si beam. This can be simply understood as the linear lattice expansion coefficient of GaAs is very similar to that of Ge.

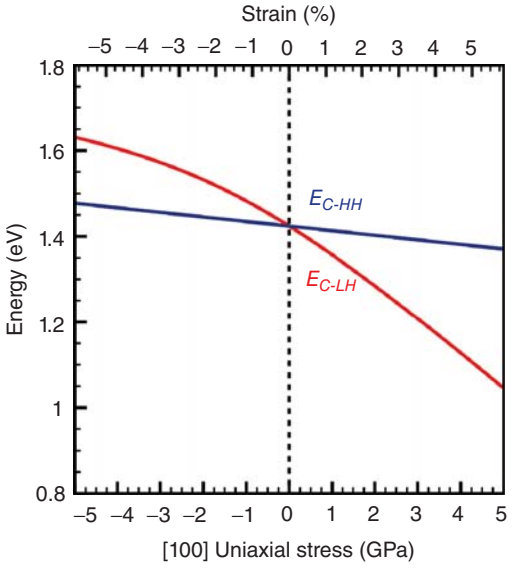

Figure 10.9 Uniaxial strain versus bandgap of GaAs.

Figure 10.10 Cross-sectional TEM image of GaAs on Ge on off-cut SOI.

Figure 10.11 shows PL spectra with and without stressing. It is clearly shown that GaAs PL peak is red-shifted by stressing the beam at the top. Releasing stress completely restored the PL spectrum before stressing. This proved that the red-shift should be induced by elastic deformation due to tensile stress and not by the defect due to plastic deformation of GaAs.

Those results obtained from the various beams of (i) Si, (ii) Ge on Si, and (iii) GaAs on Ge on Si, have proven that strain in semiconductors is an excellent entity to engineer/tune the bandgaps.

To implement the beam structure on a chip, we have studied the use of electrostatic bending instead of mechanical force bending [11]. Applying a voltage across the beam and base Si of SOI has demonstrated bending [12].

In this section, we have demonstrated that strain is an enabler to tune the bandgap of a semiconductor, using one dimensional beam structures. It is also clear that two dimensional strain is more effective to modulate bandgap as

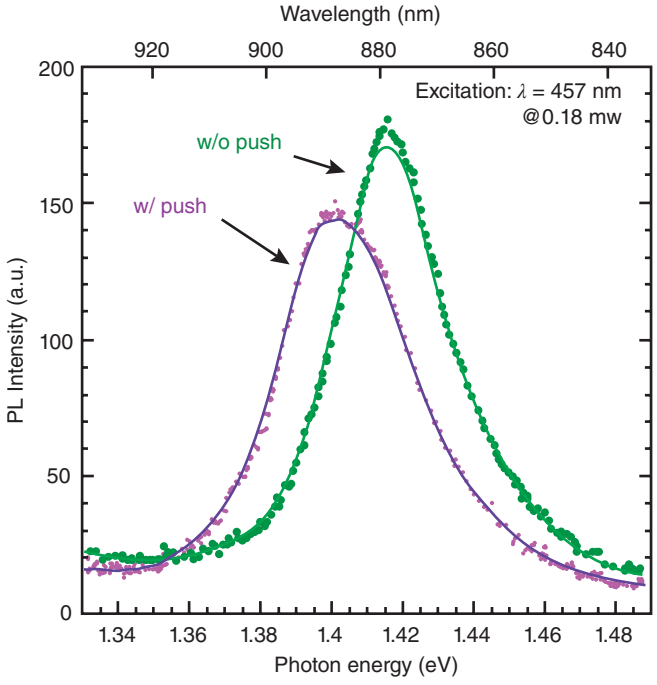

Figure 10.11 Photoluminescence spectra of GaAs on Ge on SOI with and without strain.

illustrated in Figures 10.1 and 10.6. One way to strain semiconductors has been reported [13].

10.4 Strain-Engineered Tunability of Lasers

In the final section, we like to discuss the ultimate goal of the strain-engineering of light emitters. Figure 10.12 shows two dimensional strain versus bandgap relation of GaAs, and the whole wavelength range currently being used in optical fiber communication, O- to U-band (1260 – 1675 nm). It is clear that GaAs can be tuned to emit the whole wavelength being used in fiber optics. This indicates that one material- based light emitter can cover the wavelength range under strain control. Light emitters are one of the notable power consumpters. To reduce it, there have been various advanced approaches, such as structures based on microresonators, architectures referred to as laser sleeping, and so on. This approach presented in this chapter, that is, strain-tunable light emitter can be another candidate for the power reduction. The pros are that only one light emitter is enough to integrate on a chip. The implementation requires a new algorism to utilize one wavelength at one time. Thus, we may need a couple of light emitters instead of one to meet the requirement. However, it is definitely effective to reduce the power consumption

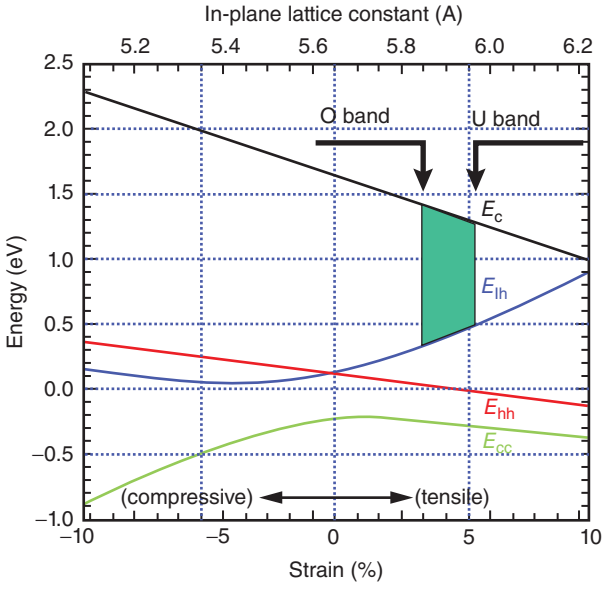

Figure 10.12 Two dimensional strain versus bandgap relation of GaAs.

with an advanced algorism for this. The advanced algorism should be an extrapolation of the laser sleeping algorism that has been extensively studied recently. The amount of strain required to tune the whole wavelength is around 5% when GaAs is used as the material. However, the material should be lower bandgap materials such as InGaAsP whose bandgap is the center of the whole wavelength range, ~1450 nm. Then, the strain required to tune the bandgap in the whole range is reduced substantially, ranging from −1.5 to +1.5%. It is worth mentioning that the amount of tensile strain has been demonstrated for the Si beam structure [8].

10.5 Conclusions

WDM is indispensible for Si photonics to increase the bandwidth density on a chip. Ge is the key material to implement WDM on a chip because it functions as light emitter, modulator, as well as photodetector on a Si CMOS platform. Bandgap engineering of group IV semiconductors is not trivial because of the large mismatch of lattice constant and indirect bandgap nature. In this chapter we have focused on strain tuning on the bandgaps of Si, Ge, and GaAs on a Si CMOS platform. The devices used here are of cantilever structures and the stress applied is in one-dimension. It has been shown that their bandgaps are clearly shrunk under tensile strain applications which has been reproduced by the kp theory with deformation potentials. This evidently shows a proof of concept that strain engineering of Ge can be implemented on a Si CMOS platform. Finally, we have discussed that

strain-tunable light emitters could cover the whole wavelength range of optical fiber communication

Acknowledgment

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11
Ge Quantum Dots-Based Light Emitting Devices

Xuejun Xu, Takuya Maruizumi, and Yasuhiro Shiraki

11.1
Introduction

The communication traffic in the Internet is exploding fast and demands for higher transfer and processing speeds require extremely high power consumption. But much of this energy is dissipated in electrical links and computing processors due to the resistive metal interconnect, which impedes both data transmission rate and energy efficiency.

Optical interconnect technology to avoid these problems has been extended from long- distance communication to on-chip optical interconnection by adopting silicon photonics technology compatible with the complementary metal oxide semiconductor (CMOS) platform. The most crucial component in silicon photonics is the light source; however, silicon-based light emitter is still under development due to the inherent property of indirect band gap of silicon. Although the recent engineering approach to circumvent this issue is the convergence of III – V materials for light emitter and Si for CMOS platform, much more effort to develop silicon-based light emitter technology has to be continued to establish true silicon photonics. So far, numerous approaches have been adopted to develop room temperature silicon light emitting source with high efficiency. Among these, Ge self-assembled quantum dots (QDs) embedded in a small optical cavity is one of the most promising candidates for light source due to its advantages of full compatibility with Si CMOS technology and also its strong light emission in the telecommunication range.

In this chapter, the formation of Ge QDs on Si substrate and their luminescent properties are reviewed first, then fabrication process and performance of light emitting devices composed of Ge QDs and a small optical cavity are described. Two types of optical cavities are included. One is the standing-wave-type resonator such as a photonic crystal (PhC) cavity. The other is the traveling-wave-type resonator such as a microdisk/microring resonator with whispering gallery resonance mode. Finally, state – of-the-art current-injected light emitting diodes (LEDs) with Ge QDs embedded in PhC nanocavities and microdisks are discussed in detail.

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11.2
Formation of Ge Dots on Si Substrates and Their Luminescent Properties

For the first time, the formation and luminescence of Ge dots on Si substrates were reported by two groups in 1995 [1, 2]. Since then, a large number of studies on Ge dot formation and optical properties of Ge dots have been conducted. As there are several good reviews [3–7] concerning Ge dot formation, some general features of the formation are described here [8].

The formation and luminescence of Ge dots were observed when quantum wells (QWs) of Si/pure–Ge/Si were formed on Si substrates and the thickness of the well was increased above the so-called critical thickness. As the lattice constant of Si and Ge is different, about 4.2%, the pseudo-morphic growth of Ge layers on Si substrates is limited by the accumulation of the strain energy originating from the lattice mismatch and the thickness where the strain is released by introducing misfit dislocations and/or the morphological change called "critical thickness." Figure 11.1 shows the thickness dependence of photoluminescence (PL) spectrum from Si/pure–Ge/Si QWs [1]. When the thickness of the Ge well layer is small, the PL shows a conventional quantum confinement effect of QWs and the peaks coming from the QW is seen to shift to lower energies with increasing thickness. Here, the two sharp peaks are known as no-phonon line and its phonon replica and are characteristic of indirect band-gap QWs. Above 3.7 ML, however, the peaks originating from QWs stop the energy shift and a new broad peak is seen to appear. The

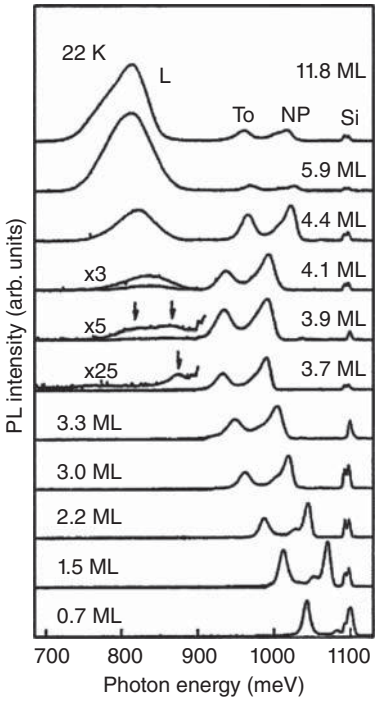


Figure 11.1 Thickness dependence of PL spectrum from Si/pure–Ge/Si quantum wells. Reprinted with permission from [1], Copyright [1995], AIP Publishing LLC.

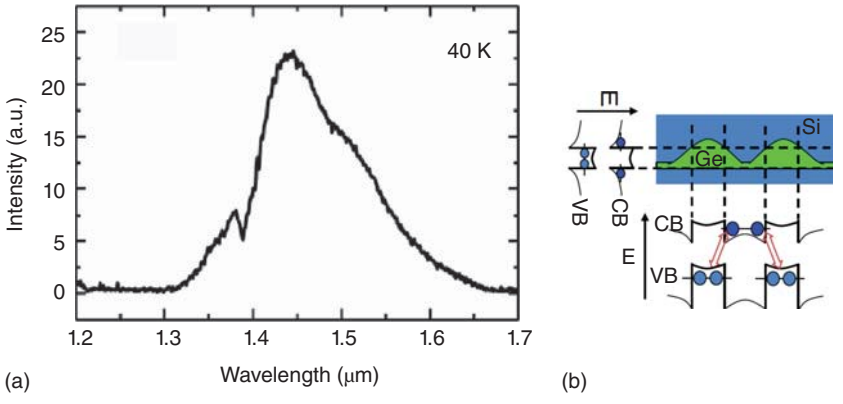


Figure 11.2 A typical PL spectrum of Ge quantum dots grown on Si substrates (a) and a schematic showing luminescence transition occurring in Ge dots (b).

appearance of this broad peak was revealed to well correspond to the formation of Ge islands observed by transmission electron microscopy (TEM) measurements. From the PL spectrum where two kinds of PL exist, we can say that above the critical thickness, Ge begins to form luminescent islands on the Ge wetting layer providing sharp PL peaks in order to release the accumulating strain energy.

Figure 11.2a shows a typical PL spectrum of Ge dots grown on Si substrates and Figure 11.2b is the schematic that shows luminescence transition occurring in Ge dots. Because the band alignment of Ge dot and Si matrix is spatially indirect, electrons and holes are separately confined in Si conduction and Ge valence bands, respectively, and the radiative transition occurs indirectly in the space. The asymmetric broad peak is thought to be composed of two peaks, that is, the no-phonon line and its phonon replica as those seen in the case of Si/Ge QWs. Here, the dip around 1.4 μm should be noted to come from water vapor absorption in the measuring system and is not essential for the Ge dot luminescence. Although it is remarkable that Ge dots give rise to significant luminescence, the fact that the luminescence peak is much broader than that of QWs indicates that the size distribution of dots is very large. In the following discussions, we shall overview the formation and their morphology of Ge dots on Si substrates.

It is well known that the Ge dot formation takes place in bimodal way; that is, small pyramidal-shape and large dome-shape dots are formed simultaneously as shown in Figure 11.3 and that the relative number changes depending on the growth conditions. When the growth temperature is decreased, the number of dots becomes larger and the size becomes smaller, particularly the density of pyramids becomes bigger than that of domes. At lower temperatures, domes and pyramids disappear and a quite large number of small elongated dots known as "hut-clusters"" appear as seen in Figure 11.3c. Energetically, domes are stable and pyramids are metastable and, therefore, they appear at rather higher temperatures. When the growth temperature is low, on the other hand, atom migration is suppressed and unstable hut-clusters are formed.

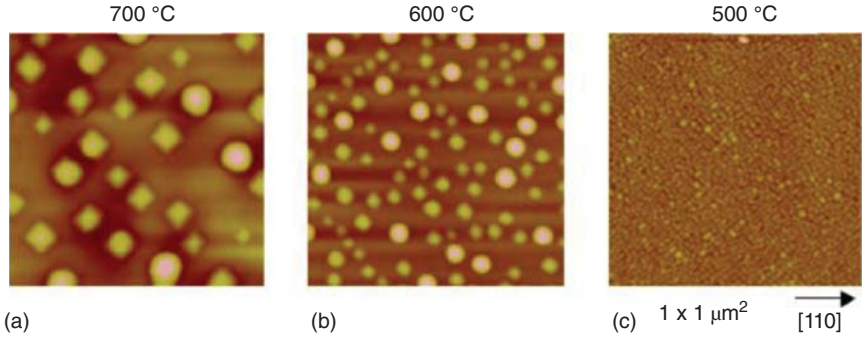


Figure 11.3 Atomic force microscopy (AFM) images of Ge dots grown at (a) 700°C, (b) 600°C, and (c) 500 °C. Reprinted from [3], Copyright (2005), with permission from Elsevier.

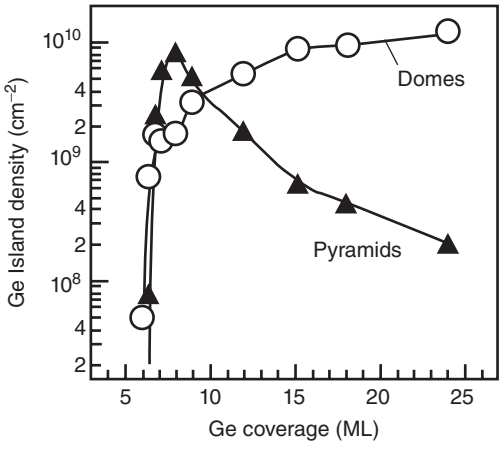


Figure 11.4 Ge coverage dependence of island density. Reprinted from [3], Copyright (2005), with permission from Elsevier.

It is noted that the morphological change occurs from pyramidal shape to dome shape when the coverage is increased as shown in Figure 11.4. This is probably due to the accumulating strain. As the dome has a much larger degree of the strain relaxation than pyramids, the shape change may occur to reduce the total energy and it dominates at higher coverage.

The relative number of pyramids to domes is also dependent on the growth rate. The density of pyramids is drastically decreased by decreasing the growth rate and it is also found that inserting the growth interruption or annealing decreases the number of pyramids. This reflects that the dome is energetically stable than that of the pyramid and that the shape change takes place more easily under near-equilibrium conditions.

The formation of SiGe alloy dots is also important from the point of view of device applications. At the same growth temperature, a large number of pyramids are formed in the case of SiGe dots compared to pure-Ge islands and the

domes are hardly observed. The number of pyramids increases with increasing SiGe coverage in contrast to the pure-Ge and the shape change does not take place. This feature is, however, very similar to that of the low temperature growth of pure-Ge dots where hut-clusters are formed and the shape change does not occur. On the other hand, if the growth of SiGe dots is performed at higher growth temperatures, the very similar behavior to that of pure-Ge dots aforementioned is seen to take place. That is, bimodal growth of islands and the shape change are clearly seen for SiGe islands. This similarity suggests intermixing of Si and Ge even for the pure-Ge dot formation. It is now known that the intermixing effect of Si and Ge particularly at high temperatures is important for the dot formation and it reduces the formation barrier of dots, resulting in the smaller critical thickness than that of the low temperature growth.

In some cases of device applications, Ge dots should be formed on the strained SiGe layers fabricated on Si substrates. Although the critical thickness for dot formation is different from that on Si substrates, the behavior of the bimodal growth and the shape change is very similar to that on Si. The Ge coverage dependence of the dot density is just shifted to the lower coverage, which can be understood if we consider the strain energy of the two-dimensional (2D) underlying strained layers. That is, the strain energy accumulating in the Ge layer corresponding to the Ge thickness difference for dot formation between SiGe and Si substrates is almost equal to that of the underlying strained SiGe layer. This implies that the strain of the underlying layers also contributes to the dot formation and that when the total strain of the SiGe underlying layer and Ge layer exceeds the critical one, dots begin to appear.

Stacking of dot layers is a practical way to fabricate devices and, therefore, it is important to know how the dot formation proceeds in stacks. As mentioned above, the strain originating from the underlying layer affects the dot formation very much. Therefore, if the thickness of the separation layers is properly selected, it is well known that the dots are aligned vertically as shown in Figure 11.5. This is because the strain coming from the underlying dots provides the energetically favorable sites for the dot formation. However, it should be noted that the kinetics is very complicated and the dot alignment not always occurs, that is, the dot

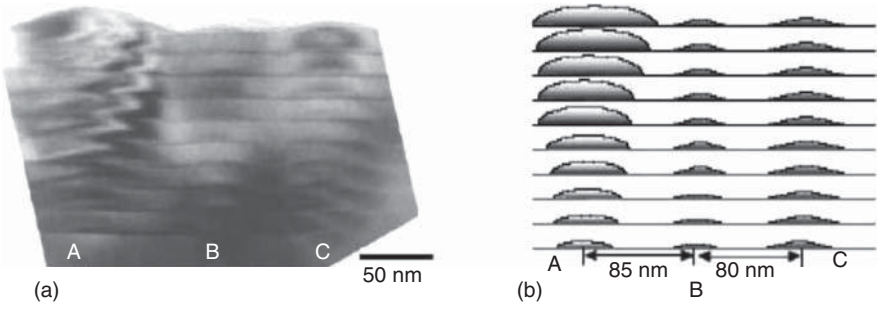


Figure 11.5 TEM image of stacked Ge dots with 10 nm Si spacer (a) and their schematic illustration (b). Reprinted from [3], Copyright (2005), with permission from Elsevier.

formation strongly depends on the growth conditions, dot distribution, and the distance from the underlying dot layer [9]. For instance, the distribution of dot size and position depends on the Si interlayer thickness. When the Si spacer is thick, the distribution is almost similar to that of single layer formation, because the strain effect of the underlying layer does not reach the upper surface. It is seen that in the sample of thinner Si spacer layer, the very large size distribution and the drastic increase of dome size appear. However, in the case of intermediate thickness, it is quite interesting that very uniform distribution and ordering of dots are realized. This tendency is also understood in terms of change of strain distribution due to the underlying dots with the spacer thickness.

Next we shall discuss how to reduce the size distribution of Ge dots. One of the powerful ways to control their size and position is to combine selective epitaxial growth and lithography [10, 11]. Gas source molecular beam epitaxy (GSMBE), where gas chemicals such as Si_2H_6 and GeH_4 are used as molecular sources instead of solid sources, has an advantage to provide selectivity in the epitaxial growth between Si and SiO_2 surfaces and Ge dots can grow only on Si surfaces.

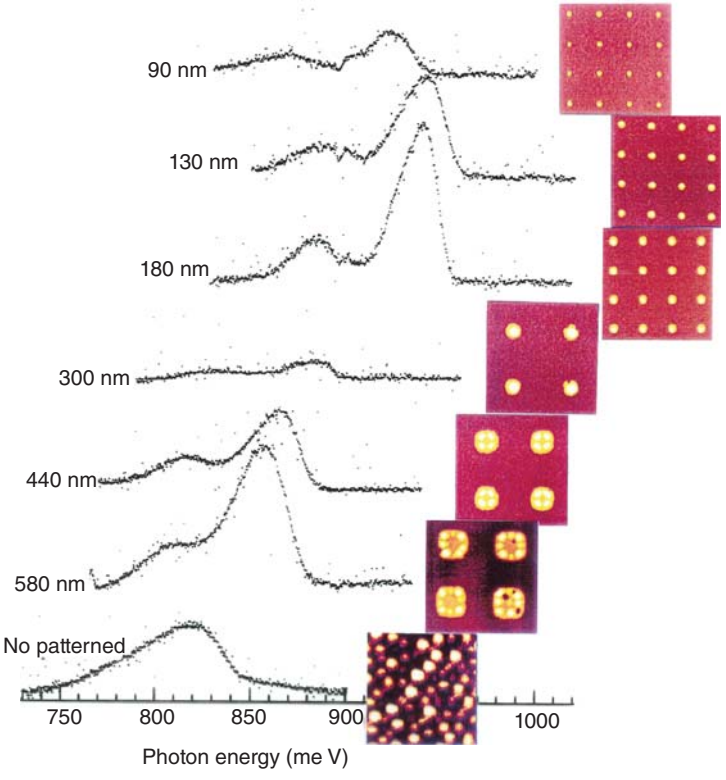


Figure 11.6 SEM images of Ge dots grown by GSMBE on Si substrate through SiO_2 patterned windows and their size-dependent PL spectrum. Reprinted with permission from [10], Copyright [1998], AIP Publishing LLC.

Therefore, when windows are opened in SiO_2 films on Si substrates, Ge dots are formed only in the window. If the window size is smaller than the Ge migration length, only one Ge dot grows in a window and the dot size decreases with decreasing window size [10]. These controlled Ge dots give rise to luminescence and well-resolved two peaks are observed in contrast to the disordered Ge dots as shown in Figure 11.6.

In order to enhance the quantum effect of Ge dots, there are several attempts to reduce Ge dot size and increase the dot density. Pre-deposition of elements such as C [12, 13] and B [14] is shown to be very effective in reducing the size. Incorporation of C is found to be also effective when the dots are formed by using GSMBE [15]. When $(CH_3)_3SiH(TMS)$ is incorporated in the GeH_4 gas, some interesting features different from pure-Ge dot formation with GeH_4 are seen. That is, (i) the critical thickness of dot formation increases, (ii) the dot strongly reduces its size and increases the number as high as three times of the pure-Ge dots, and (iii) monomodal formation of dome-like dots occurs instead of the bimodal formation of pure-Ge dots. The dots with C provide luminescence as well, but the peak shift against the deposition is different from that of Ge dots grown at the same growth temperature and very similar to the behavior of the Ge dots at lower growth temperatures. This indicates that the migration of atoms is impeded by the presence of C atoms and, therefore, the low temperature growth mode occurs even at higher temperatures. This well corresponds to the small dot formation coming from the reduction of the migration length of atoms on the surface.

11.3
Enhanced Light Emission from Ge QDs Embedded in Optical Cavities

Although many efforts of material engineering have been proposed and demonstrated to increase the light emission efficiency of Ge self-assembled QDs, it is still rather low for the practical application due to the weak localization potential of Ge QDs. Usually, the luminescence can be only observed at cryogenic temperatures. On the other hand, it is well known that the spontaneous emission rate (SER) of light emitters is not only related to the transition strength between bands, but also strongly affected by the photon density of states where the emitters are located, according to the Fermi's golden rule. This gives us opportunities to enhance the light emission by modifying the electromagnetic environment around the emitters.

Particularly, optical cavity is an efficient tool to manipulate the SER. According to the Purcell effect, by embedding light emitters inside the optical cavity, the SER can be enhanced by a factor of

$$F_P = \frac{3}{4\pi^2}\left(\frac{\lambda_c}{n}\right)^3 \frac{Q}{V},$$

where λ_c is the resonant wavelength of the cavity, n is the refractive index of the material, Q and V are the quality-factor (Q-factor) and mode volume of the cavity,

respectively. This effect was first proposed by E. M. Purcell at radio frequencies in 1946 [16], and was applied to optical frequencies soon [17–21]. Based on this effect, enhanced SER has been observed in a variety of material systems with optical cavities, such as InAs QDs [22, 23], CdSe QDs [24], Si nanocrystals [25, 26], Si-rich SiN [27], Si crystal [28, 29], and so on.

In order to obtain a large Purcell factor, optical cavities with high Q-factor and small mode volume are required. Owing to the large refractive index contrast between Si and SiO_2/air, the cavities can be scaled down to micrometer (microcavities) or nanometer (nanocavities) sizes, while still preserving high Q-factors. Two types of such cavities are used in our work: 2D PhC cavity, and whispering gallery mode (WGM) resonators, including microdisk and microring. 2D PhC cavity is formed from PhC slab with periodic holes on a dielectric slab. The cavity modes are confined by PhC band gap in the plane of the slab and by total internal reflection (TIR) between core and cladding materials perpendicular to the slab. On the other hand, WGMs supported in microdisk/ring travel in a circle along the disk/ring edge and are confined by TIR both in the in-plane and out-plane directions. In order to realize vertical optical confinement, silicon-on-insulator (SOI), instead of Si, are used as the substrate to grow Ge QDs.

In the following two sections, we will review some of our recent results on enhanced light emission from Ge QDs embedded in different types of optical cavities at room-temperature.

11.4 Optically Excited Light Emission from Ge QDs

In order to excite the light emission from Ge QDs, carriers should be injected and radiatively recombined. Optical pumping by a laser with shorter wavelength (higher energy), which can be efficiently absorbed by the Ge QDs and host Si, is the easiest way for excitation.

11.4.1 Photonic Crystal Cavity

11.4.1.1 General Device Description

The schematic diagram of PhC cavities is shown in Figure 11.7. Single or multiple layers of Ge QDs are grown on SOI wafer with a thin top Si layer by MBE, and the PhC patterns are usually defined by electron beam lithography (EBL) and dry etching. The light emission properties of these devices are usually characterized by PL. Figure 11.8 shows a typical setup of a confocal microscopy photoluminescence (μPL) system. The excitation is done by a pumping laser with shorter wavelength, for example, 532 nm. The excitation laser is focused onto the cavity with a micron spot size by an objective lens. The luminescence signal is then collected and dispersed by a monochromator and detected by a detector with high sensitivity in the wavelength range of Ge QDs light emission.

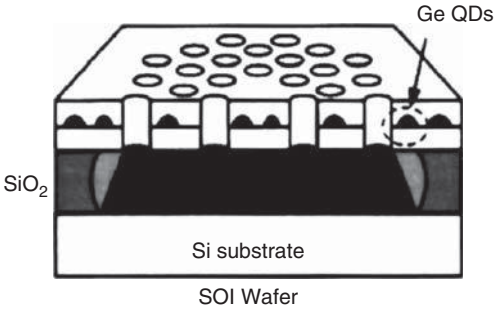


Figure 11.7 Schematic diagram of the PhC cavity on SOI wafer containing Ge QDs. Reprinted with permission from [32], Copyright [2006], AIP Publishing LLC.

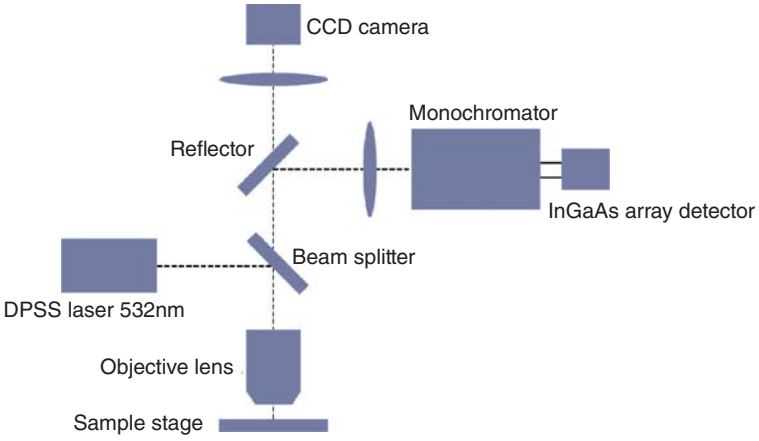


Figure 11.8 Typical setup of a confocal microscopy photoluminescence (μPL) system.

11.4.1.2 PL from PhC Microcavities

The first demonstration of enhanced PL from Ge QDs by PhC microcavities was reported by David *et al.* at 2003 [30]. By creating defects in 2D PhC on SOI containing Ge QDs to form H2-, H3-, and H5-type cavities, they observed dramatic enhancement of 1.3 – 1.5 μm room-temperature emission and nonlinear evolution with pumping power [31]. However, the pumping power they used to obtain the luminescence is relatively large, on the order of several tens of milliwatts. And also, no clear resonance was observed in their spectra.

Our group then first demonstrated strong resonant PL from Ge QDs in a free-standing H2-type PhC microcavity at room-temperature [32]. The scanning electron microscopy (SEM) image of the cavity is shown in Figure 11.9a, and the PL spectrum from an H2-type cavity with lattice constant of $a = 540$ nm and hole radius of $r = 225$ nm is shown in Figure 11.9b. The power of the incident excitation laser was only 0.19 mW. Spectrum recorded in the unprocessed region on the same chip with the same excitation power, which is denoted as a reference, is

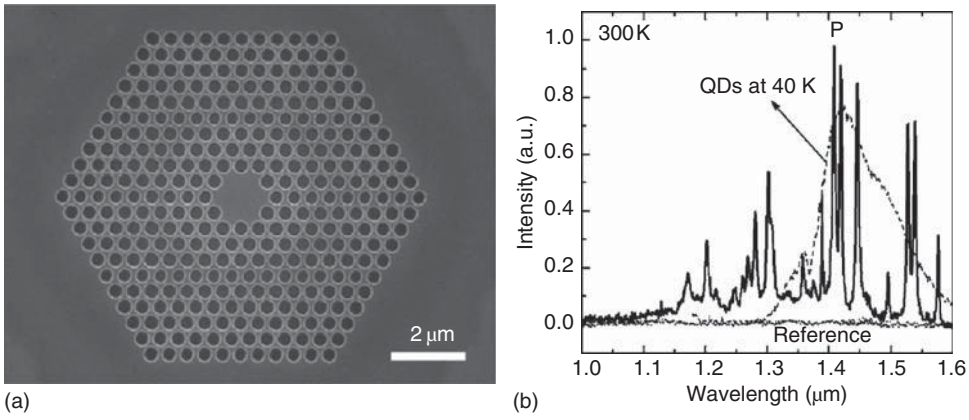


Figure 11.9 (a) SEM image of a typical fabricated H2-type cavity. (b) PL spectrum from an H2-type cavity with lattice constant of $a = 540$ nm and hole radius of $r = 225$ nm. Reprinted with permission from [32], Copyright [2006], AIP Publishing LLC.

also shown in the figure. Owing to the very low optical yield and the low detector sensitivity, a clear spectrum is not obtainable for the unprocessed Ge QDs at room-temperature and, therefore, the spectrum measured at 40 K is plotted to show the spectrum shape of the Ge QDs. Multiple sharp resonant peaks are clearly observed from 1.2 to 1.6 μm, showing a strong optical resonance inside the cavity. Significant enhancement of the luminescence intensity is also achieved compared with the reference. The full width at half maximum (FWHM) of the resonant luminescence peak at 1.58 μm is 2.8 nm, from which a Q-factor around 560 is deduced. The presence of these strong resonant peaks also suggests that the luminescence in the Ge dot-based system is not quenched by the electronic defect states at the interfaces generated by the fabrication process.

A super-linear evolution of the PL intensity against the pumping power is also shown in our devices. Figure 11.10 shows the power dependence of the luminescence peak (denoted as P in Figure 11.9b) intensity at 1.41 μm. The possible reason for the rapid increase is the three-dimensional (3D) carrier localization. In normal direction, the carriers are confined by the Si slab, while the lateral PhC pattern partially inhibits lateral diffusion of the carriers. This leads to local dense electron-hole plasma, which provides an additional scattering mechanism for the carriers to the zone center and enhances the PL. Moreover, at high carrier density, strong band bending occurs around the Ge/Si heterostructure and the overlap between electron and hole wave functions is enhanced, resulting in the enhancement of the luminescence efficiency. Because the trapping of holes in Ge islands is also strengthened, the carrier diffusion to parasitic nonradiative recombination centers is limited, which also contributes to the enhancement of the luminescence.

11.4.1.3 PL from L3-Type PhC Nanocavities

In the above work, SOI wafer with a 70-nm-thick top Si and 400-nm-thick buried silicon oxide (BOX) was used as the substrate to grow Ge QDs. Owing to the thin

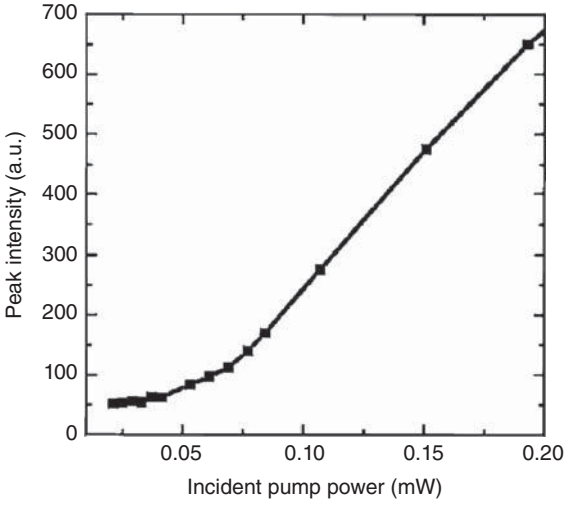


Figure 11.10 Pumping power dependence of the peak intensity at 1.41 μm, denoted as P in Figure 11.9b. Reprinted with permission from [32], Copyright [2006], AIP Publishing LLC.

BOX layer, the Si substrate beneath the BOX induces large effects on the optical performances of the cavities, that is, large leakage loss to the substrate limiting the Q-factors of the cavities. In order to reduce the effect of substrate, SOI wafer with a thicker BOX is required. On the other hand, in order to ensure the single-mode guiding of the top Si/Ge layer after growth of Ge QDs, its thickness should be thin enough, typically, 200–300 nm. However, SOI wafers with very thin top Si layer and thick BOX layer are not commercially available. Therefore, in the following work, we turn to use SOI wafer with 160-nm-thick top Si and 2-μm-thick BOX, which is the SOI wafer with the thinnest top Si layer and thick BOX that we can get. The top Si is still too thick for our application. Therefore, the top Si layer is first thinned to around 50– 60 nm by thermal oxidation and wet etching by hydrofluoric acid solution. Then, the threelayers of Ge QDs with Si spacers and cap layer are grown on top. The total thickness of Si/Ge layer is from 180 to 260 nm, dependent on the growth conditions.

Figure 11.11a shows the PL spectrum of a free-standing L3-type PhC nanocavity with incident excitation power of about 2 mW, together with its SEM image in the inset [33]. The L3-type PhC nanocavity is formed by removing three holes along the Γ-*K* direction of a hexagonal PhC pattern [34]. Several sharp resonant peaks are clearly observed in the wavelength range from 1.2 to 1.6 μm.

The resonant peaks in the spectrum are identified to the PhC cavity modes by numerical simulation based on plane-wave expansion and 3D finite-difference time-domain (FDTD) methods. The calculated photonic band is shown in Figure 11.11a by the shaded area. All of the resonant peaks are located inside the band gap. Five cavity modes are found in the photonic band gap. The resonant wavelengths are shown in Figure 11.11a as the red dashed lines. They agree well with the experimental PL results. The resonant peak with the longest wavelength,

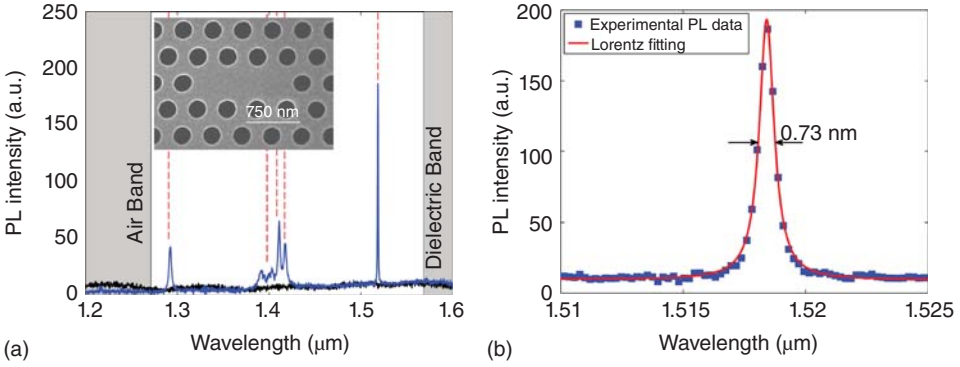


Figure 11.11 (a) PL spectrum of a free-standing L3-type PhC nanocavity; the inset shows the SEM image of the cavity. The lattice constant a is 423 nm and the hole radius r is 126 nm, measured from the SEM image. (b) Lorentz fitting of the resonant peak corresponding to the fundamental cavity mode. © [2012] IEEE. Reprinted, with permission, from [33].

which corresponds to the fundamental cavity mode, has a Q-factor of about 2000 through Lorentz fitting, as shown in Figure 11.11b. The Q-factor is smaller than the simulation value (~4000). The deviation mainly comes from the extra loss induced by the roughness in the air holes formed by fabrication and free-carrier absorption by excitation laser.

The properties of light emission are strongly dependent on the excitation conditions and structure parameters of the cavity. Figure 11.12 shows the peak wavelengths, Q-factors of the fundamental cavity mode of a L3 PhC nanocavity

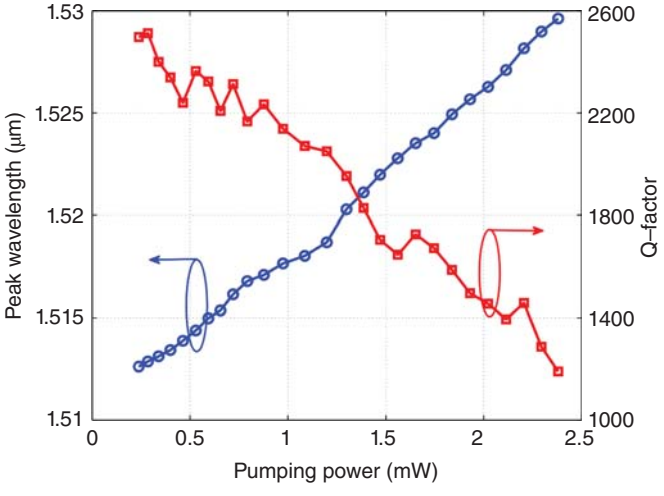


Figure 11.12 Peak wavelengths and Q-factors of the fundamental cavity mode of a L3 PhC nanocavity with $a = 440$ nm and $r = 0.28a$ extracted from the PL spectra under different pumping powers. © [2012] IEEE. Reprinted, with permission, from [33].

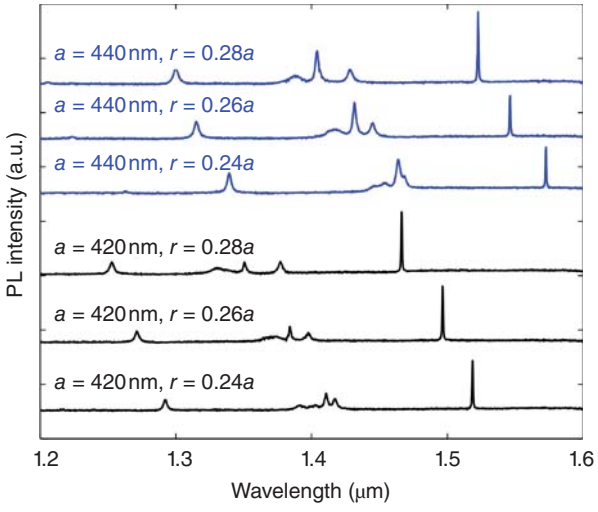

a = 440 nm, r = 0.28a
a = 440 nm, r = 0.26a
a = 440 nm, r = 0.24a
a = 420 nm, r = 0.28a
a = 420 nm, r = 0.26a
a = 420 nm, r = 0.24a
PL intensity (a.u.)
1.2
1.3
1.4
1.5
1.6
Wavelength (μm)

Figure 11.13 PL spectra of L3-type PhC nanocavities with different lattice constants and hole radii. © [2012] IEEE. Reprinted, with permission, from [33].

extracted from the PL spectra under different pumping powers. As the pumping power increases, the resonant peak is shifted to a longer wavelength. This red-shift comes from the increase of the refractive index of Si due to the heating effect of the pumping laser. The wavelength shift is almost linear with the pumping power in the range we used. We also observe the Q-factor decreasing against the pumping power. This is due to the increased free-carrier absorption [35].

L3 PhC nanocavities with different lattice constants and hole radii were also characterized to study the dependence of light emission properties on the geometric parameters. The PL spectra are shown in Figure 11.13, with their designing parameters nearby. As the lattice constant varies from 420 to 440 nm and the hole radius varies from $0.24a$ to $0.28a$, the PL spectra show similar shape and peak number, indicating that the mode structure of the cavity does not change. In the meanwhile, all of the peak positions are shifted to longer wavelength as the lattice constant increases and to shorter wavelength as the hole radius increases. This is reasonable because the effective refractive index of a single period is increasing as the lattice constant increases and hole radius decreases. The wavelength shift is almost linear with the lattice constant and hole radius in the range we used. The geometric-parameter-dependence provides an efficient way to tune the light emission wavelength. Through carefully designing the parameters, the emission wavelength can be adjusted in a very large range from 1.3 to 1.6 μm.

Compared with that obtained from unprocessed region, the light emission intensity from the PhC nanocavity is significantly enhanced at the resonant wavelengths. This enhancement is attributed to two factors: one is the enhanced SER of Ge QDs inside the cavity and the other is the enhanced light extraction efficiency. In order to increase the light emission efficiency further, either of the Purcell factor and light extraction efficiency should be increased. The light extraction

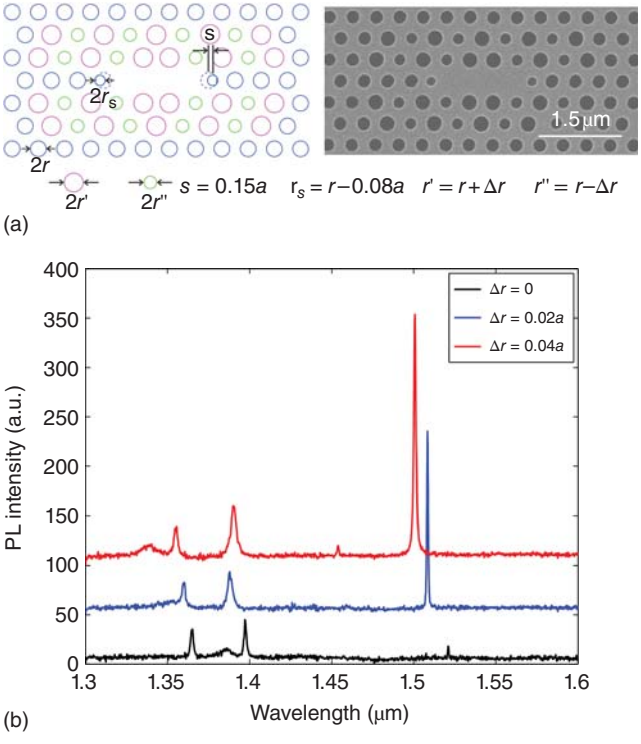


Figure 11.14 (a) Schematic diagram of a modified L3-type PhC nanocavity with far-field optimization, together with the SEM image of the fabricated cavity. (b) PL spectra of the L3-type PhC nanocavities with and without far-field optimization. The lattice constant is 420 nm and hole radius is 0.26*a*. © [2012] IEEE. Reprinted, with permission, from [33].

efficiency is related to the overlap between the far-field pattern of the cavity mode and the collection optics. An objective lens usually has a limited numerical aperture (NA), which can only collect the light radiation within a small angle. So the easiest way to increase the light extraction efficiency is to turn the far-field pattern more concentrated along the vertical direction. Optimization of far-field pattern is performed by modifying the radii of holes around the cavity [36]. As one can see in the schematic diagram and SEM image in Figure 11.14a, the radii of holes around the cavity are increasing and decreasing one by one by a quantity of Δr. In this way, a double-period perturbation is applied to the cavity. The field distribution at the first Brillouin zone boundary ($k = 2\pi/a$) in the reciprocal space will be folded back to the Brillouin zone center ($k = 0$). So the far-field pattern will be more concentrated along the vertical direction. Figure 11.14b shows the PL spectra from PhC nanocavities with and without far-field optimization. The objective lens used here has an NA of 0.50. As Δr increases, the PL intensity for the fundamental cavity mode has a large enhancement, as expected.

11.4.1.4 PL from Double-Heterostructure PhC Nanocavities

Besides L3-type, several other types of PhC cavities can also be used to enhance the light emission from Ge QDs [37]. As an extra example, the results from double-heterostructure (DH) PhC nanocavity [38] are also shown here. The DH cavity is formed based on a W1-type line defect PhC waveguide (PCW). The hole radii of the central parts of the PCW were reduced by Δr. The schematic diagram of the cavity is shown in Figure 11.15a. Figure 11.15c shows the photonic band diagrams of the PCWs with different hole radii. Owing to this difference, there is a mode gap between two PCWs and a "photonic well" is established in the central parts of the PCW, similar with that in semiconductor crystal lattices. If the central PCW is short enough, quantized frequency level will be generated in the well, corresponding to the PhC cavity mode. The mode is laterally confined by the photonic barriers, much more gently than that in point defect PhC cavities. The cavity is therefore thought to have a much higher Q-factor than point defect PhC cavities. Song *et al.* have experimentally demonstrated a passive Q-factor approaching 1 million with this type of cavity.

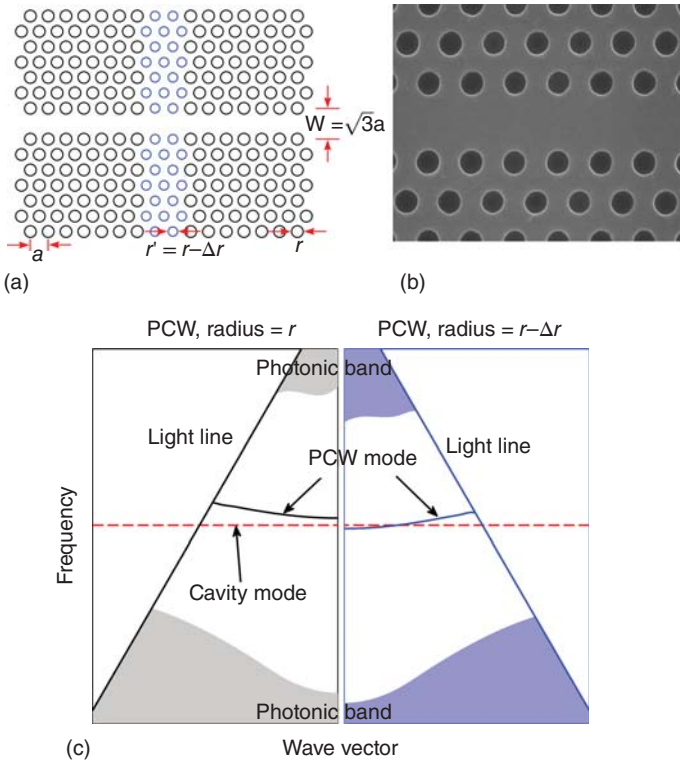


Figure 11.15 (a) Schematic diagram and (b) SEM image of the DH PhC nanocavity. (c) Photonic band diagrams of the PCWs with different hole radii of r (left panel) and $r - \Delta r$ (right panel). Reprinted from [37], Copyright (2013), with permission from Elsevier.

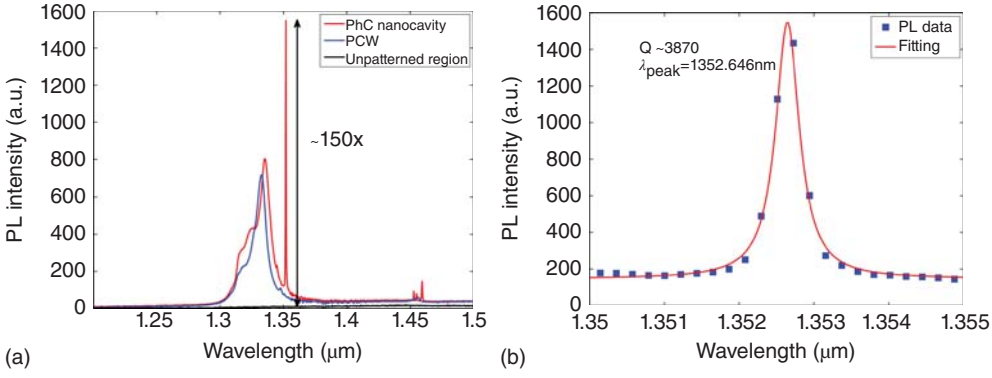


Figure 11.16 (a) PL spectra of Ge QDs embedded in the DH PhC nanocavity, PCW, and unpatterned region. (b) Lorentz fitting of the resonant peak at 1.352 μm wavelength. Reprinted from [37], Copyright (2013), with permission from Elsevier.

The SEM image of a fabricated device is shown in Figure 11.15b. The designed parameters of this cavity are: lattice constant $a = 400$ nm, hole radius $r = 0.28a$, PCW width $W = \sqrt{3}a$, and $\Delta r = 0.01a$. The hole radius difference is too small to be distinguished visually in the SEM image. Figure 11.16a shows the PL spectra recorded at the different positions of the device. A very sharp and strong resonant peak with Q-factor up to about 3870, according to the Lorentz fitting as shown in Figure 11.16b, is observed in the PL spectrum from the cavity. The resonant wavelength is around 1.352 μm, at which the PL intensity is enhanced by a factor of 150 compared with that from an unpatterned region. Besides the sharp resonant peak, a relative broad peak also appears in the PL spectrum. We confirm that this broad peak comes from the transmission band of the PCW surrounding the cavity by comparing the PL spectrum from the cavity with that from the PCW region, which is also shown in Figure 11.16a. We can also see that the peak position of the cavity mode is just located outside but very close to the transmission band of the PCW around the cavity, which is consistent with the band diagrams shown in Figure 11.15c.

11.4.2 Microdisk/Ring

11.4.2.1 General Device Description

Microdisk/ring is one of the simplest optical cavities, which has been used to enhance the SER and fabricate low-threshold small lasers for a long time. The supported WGMs can achieve very high Q-factor. Compared with that of PhC cavity, defining microdisk/ring patterns does not need accurate lithography techniques such as EBL, and are thus much easier to fabricate. The size scale of microdisk/ring is usually on the order of several tens of micrometers, or even larger in order to achieve an ultrahigh Q-factor. In a Si/SiO_2 or Si/air system, however, the refractive index contrast is very large, thus the radius can be scaled

down to a few micrometers or less while preserving high Q-factor. This is very attractive for the enhancement of SER in which small mode volume is required. The microdisks/rings are also fabricated on SOI wafer containing Ge QDs here. Unlike free-standing PhC cavities, the BOX layer is left because there was no support structure for microring and microdisk with very small diameter.

11.4.2.2 PL from Microdisks and Rings

The insets in Figure 11.17a,b show the SEM images of microdisk and microring with outer radii of 1.1 μm [33, 39, 40]. During the μPL measurement, the pumping laser spot was located close to the edge of the disk and ring in order to excite the WGMs. The PL spectra are shown in Figure 11.17. Although the WGMs' radiation is mainly along the in-plane direction and the emission angle is very small, sharp resonant peaks corresponding to WGMs are still clearly observed in the spectra recorded in the vertical direction. Thanks to the nonideal side wall of the disk or ring due to fabrication inaccuracy, the in-plane emission is scattered by the edge and thus can be collected by the objective lens on top. The measured Q-factor of these WGM resonant peaks is typically in the range of 1000–3000. This indicates that the optical confinement for these small microdisks and microrings is still very large. So we can realize both high Q-factor and small mode volume.

The WGMs are identified through comparison between peak positions in PL spectrum and numerical simulation results by FDTD. The mode index and polarization are labeled near the resonant peaks in Figure 11.17, in the form of $TE(p, m, n)$ or $TM(p, m, n)$. p is the index number of the slab mode in the vertical direction, m and n are azimuthal and radial number in plane. Through solving Maxwell equations, we can find that the slab only supports the fundamental transverse electric (TE) and transverse magnetic (TM) modes. So there are only WGMs with the

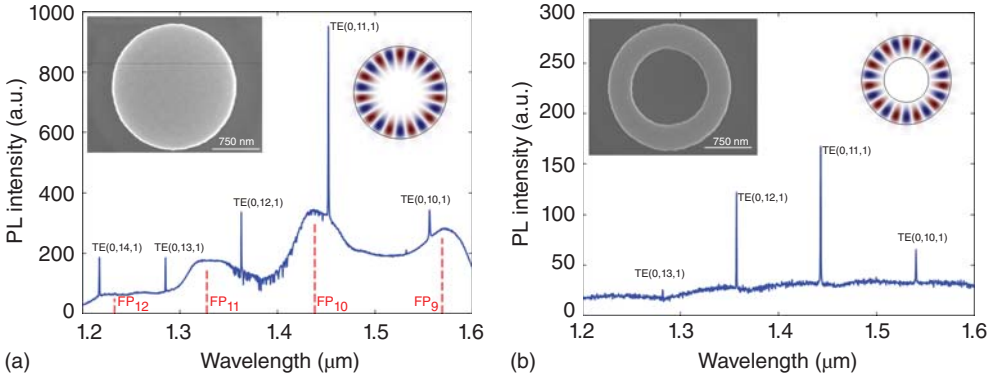


Figure 11.17 (a) PL spectrum from microdisk with outer radius of 1.1 μm, together with its SEM image and mode profile of *TE*(0, 11, 1) WGM in the inset. The mode indexes of WGMs and FP modes are also shown. (b) PL spectrum from microring with outer radius of 1.1 μm and ring width of 0.6 μm, together with its SEM image and mode profile of *TE*(0, 11, 1) WGM in the inset. © [2012] IEEE. Reprinted, with permission, from [33].

p index of 0. The mode profile for each WGM is also calculated. The indexes m and n are specified by the number of poles along azimuthal and radical directions from the mode profile. As an example, the mode profile of $TE(0, 11, 1)$ mode is shown in the inset of Figure 11.17. From the PL spectrum, we can see that only the WGMs with the lowest radial number are observed.

For microdisk, there are not only WDM-based sharp resonant peaks in the PL spectrum, but also broad peaks on the background. These broad peaks correspond to the resonances of Fabry–Perot (FP) cavity formed by the opposite edges of the disk [40]. The peak wavelengths can be calculated from the resonant condition of FP cavity $m\lambda/n_{\text{eff}}(\lambda) = 4R$, where m is the order of the FP mode, R is the radius of the disk, and n_{eff} is the effective index of fundamental TE mode of the slab. The calculated peak wavelengths are labeled as FP_m with the red dash lines in Figure 11.17a, and agree well with the positions of the broad peaks. Because the reflection coefficient at the Si/air interface is around 30%, a large amount of optical power escapes from the FP cavity when light is reflected at the disk edge. This leads to a small Q-factor. Thus, the FP resonant peaks are much broader than the WGM peaks. Another evidence for this FP resonance is that we do not observe any broad peaks in the PL spectrum of microring. Owing to the existence of the central hole, the FP cavity cannot be constructed. Therefore, only WGM-based resonant peaks are observed in the spectrum.

The dependence of the pumping power on the peak wavelength and Q-factor of the WGM modes is similar to that of PhC cavities, and are therefore not shown here . For structure parameters, the radius is a key for microdisk/ring, which determines the resonant wavelength, Q-factor, and mode volume of WGMs, thus has large effects on the light emission properties. Figure 11.18 shows the PL spectra of microdisks/rings with different outer radii. The number of WGMs increases as the outer radii of microdisk and microring. Unlike those of PhC cavities, the peak positions and free spectrum range (FSR, wavelength spacing between two successive resonant peaks) of the microdisks and microrings are determined by the optical length of the resonator, in simple, $2\pi nR$, where n is the effective refractive index

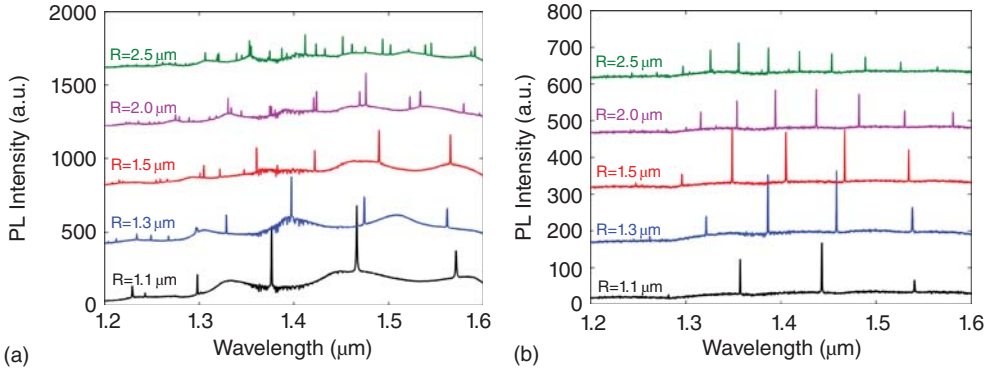


Figure 11.18 PL spectra of (a) microdisks and (b) microrings with different radii. The ring width is 0.6 μm. © [2012] IEEE. Reprinted, with permission, from [33].

of the slab mode, and R is the radius of the resonator. The larger the radius, the smaller the FSR, and there are more resonant modes in the same wavelength range. As the radius increases, the wavelength of WGM modes with the same index is also red-shifted, as in the case in PhC cavities. The Q-factor is also increased against radius due to the lower bending loss. On the other hand, the mode volume will also increase. So a compromise should be made in order to obtain a maximum Purcell enhancement factor. The optimized radius is dependent on the other parameters, such as total thickness of Ge/Si layer, sidewall roughness of the disk/ring edge, and so on. In our cases, we find that the optimized radius for microdisk is around 1.1–1.3 μm, and 1.3–1.5 μm for microring.

By comparing Figure 11.18a,b, we can see that at small radius, the peak number, and positions are almost the same for microdisk and ring with the same radius, except that all of the peaks are blue-shifted a little in the microrings. This is reasonable because an air hole inside the ring will decrease the effective refractive index of WGM. When the radius is larger, the difference between the microdisk and ring becomes larger. The PL spectrum of microring is *purer* than that of microdisk. A lot of small resonant peaks appear in the spectrum of microdisk. These peaks correspond to WGMs with high-order radial number, which can be filtered by the central holes inside the microring. Thus, the mode density per wavelength (or frequency) in the microring is much smaller than that in the microdisk. This means fewer modes can be coupled to the active medium, thus the spontaneous emission coupling ratio can be increased.

11.5 Electrically Excited Light Emission from Ge ODs

Optical excitation is an easy way to probe and verify the enhanced light emission from Ge QDs embedded in optical microcavities. However, from an aspect of practical application, current-injected light emission is more desirable. For an electrical structure, efficient carrier injection into the active region should be the first and most important requirement. Owing to the small cavity size, the carriers also need to be confined well in the cavity so that the light emission can be efficiently coupled to the cavity modes. At last, electrical structure should not impose many effects on the optical performances.

11.5.1 Photonic Crystal Cavity

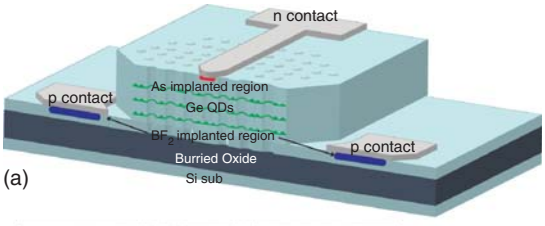
The PhC cavity usually has a micrometer or even nanometer dimension. There is rare space for the electrical structures like doping areas, contacts, and electrodes. It is thus very difficult to fabricate extra diode structure for current injection. Several complicated electrical structures have been proposed and demonstrated on III–V materials [41–44]. These structures can be also applied to our Ge QDs system.

11.5.1.1 Vertical PIN Structure

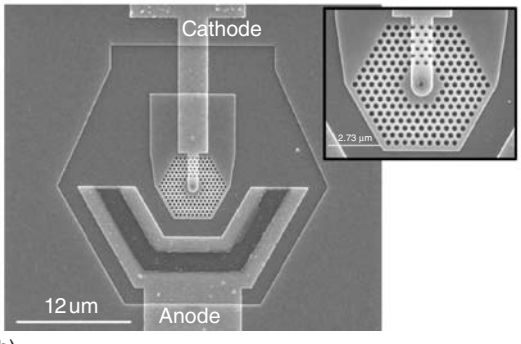
The current-injected LEDs were first demonstrated through a vertical PIN diode formed on an H3-type PhC microcavity [45]. The schematic diagram of the devices is shown in Figure 11.19a. A vertical PIN diode is integrated with the PhC microcavity, in which an N+ doping area is located on the top of the cavity and a P+ doping area is on the surrounding thin slab. In the vertical PIN diode structure, the top contact hole and electrode should be small enough to reduce their effects on the optical performances of the cavity. That is why we choose so large a cavity.

The device fabrication starts from the SOI wafer with three layers of Ge QDs and a 400-nm-thick BOX. The total thickness of Si/Ge layers was about 195 nm measured from the cross-section SEM image. The vertical PIN diode was fabricated by selective ion implantation of BF_2 and As, for P+ and N+ doping, respectively. HfO_2 was deposited on the top of the cavity to realize the upper cladding and electrical isolation. The SEM image of a fabricated device is shown in Figure 11.19b.

Figure 11.20a shows electroluminescence (EL) spectra obtained from the H3 cavity under different injected currents. Clear cavity-enhanced peaks originating from the Ge QDs are observed around the wavelength of 1.2–1.4 μm at the current larger than 50 μA. The light emission at the wavelength smaller than 1.2 μm is related to the Si band gap. As a reference, the low-temperature (40 K) PL spectrum of the Ge QDs without cavity is also shown in Figure 11.20a. Figure 11.20b shows the relationship between the integrated EL intensity and injected current, together with the current–voltage (I–V) curve of the device. We only consider the Ge-QDs



(a)



(b)

Figure 11.19 (a) Schematic diagram of the current-injected LED based on PhC microcavity with Ge QDs. (b) SEM image of a fabricated device with H3 cavity. Copyright (2012) The Japan Society of Applied Physics.

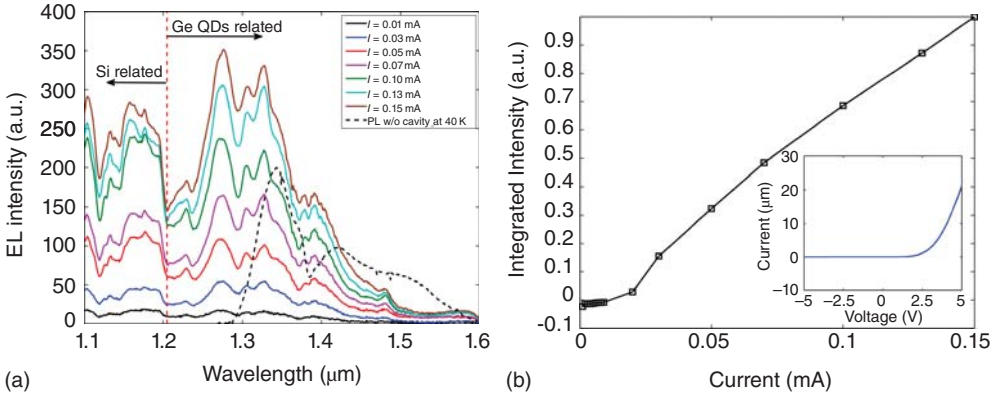


Figure 11.20 (a) EL spectra of the vertical PIN LED under different injected currents and low-temperature PL of Ge QDs without cavity. (b) Nonlinear dependence of the integrated EL intensity on the injected current. The current–voltage (I–V) curve of the device is shown in the inset. Copyright (2012) The Japan Society of Applied Physics.

related emission and the integration range starts from the wavelength indicated by the red dashed line in Figure 11.20a. The nonlinear behavior is similar to our previous results of optical-pumped devices, suggesting that 3D carrier localization also occurs in the current-injected devices.

From the EL spectrum we can see that the resonant peaks are very broad and overlapped with each other. A comparison between the EL spectrum and the PL spectrum of the device before and after HfO_2 deposition is shown in Figure 11.21a, together with the cavity mode positions calculated from FDTD simulation as the dashed lines. The resonant peaks and simulation results are in reasonable agreement, indicating that these peaks are indeed corresponding to the PhC cavity modes. Sharp peaks appear in the PL spectrum of the device before HfO_2 deposition, in which the highest Q-factor is about 150 at 1.356 μm wavelength. After HfO_2 deposition, the resonant peaks shift to longer wavelengths, due to the larger refractive index of HfO_2 than air. The Q-factor of peaks also reduces. This is attributed to the weaker optical confinement along the vertical direction. On the other hand, because the refractive index of HfO_2 is even larger than the buried SiO_2, the upper confinement is weaker than the lower. Therefore, the optics on top in the PL system can collect more radiation upward. That is why strong peaks at longer wavelength appear in the PL spectrum of the device after HfO_2 deposition.

For EL spectrum, the peak positions are not changed so much compared with those in the PL spectrum, but the Q-factor reduces a lot, and the peak number also decreases. Two reasons can be attributed: (i) Under current injection, a large portion of the current passes through the surrounding PhC area instead of the cavity region. The light emission from the Ge QDs is also enhanced by the PhC region, thus a broad background is overlapped with the resonant peaks. (ii) The metal electrode on top of the cavity induces a large absorption to the cavity modes.

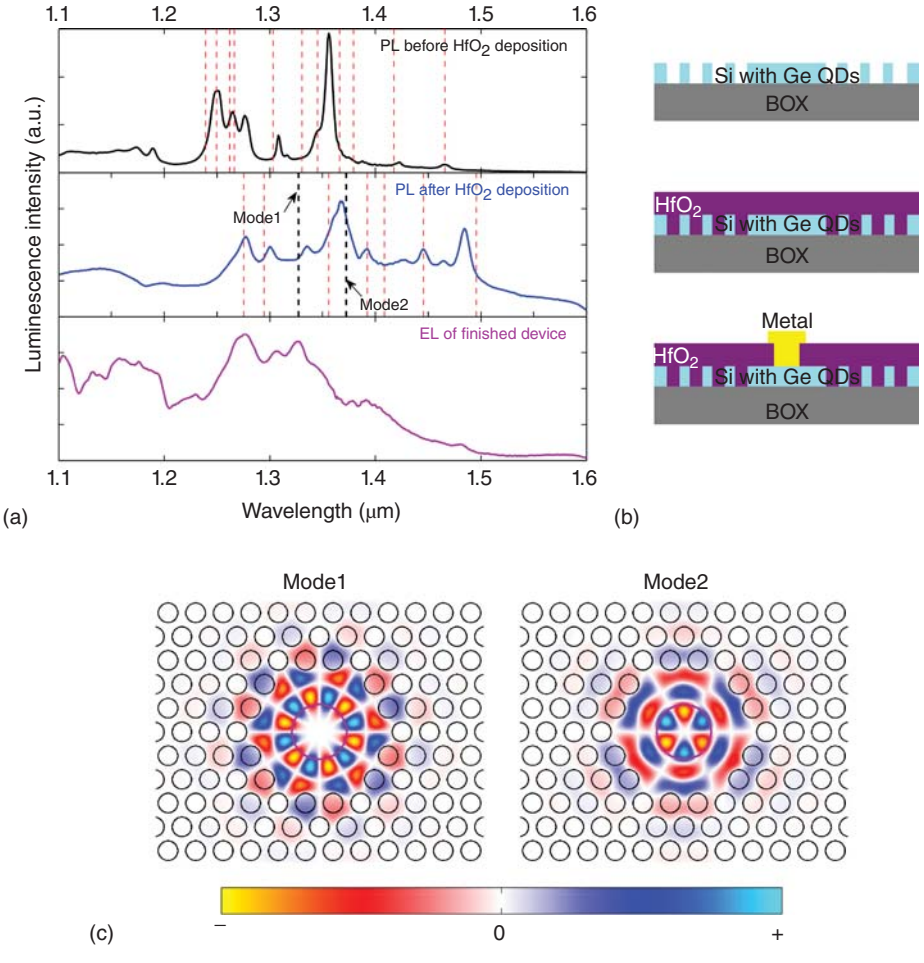


Figure 11.21 (a) Comparison of the PL spectra of the device before and after HfO_2 deposition and EL spectrum of the finished device. The cavity mode positions from the FDTD simulation results are also shown as the dashed lines. (b) Schematic diagram of the corresponding device measured in (a). (c) Field distributions of the dominant electric field component of the two modes at 1.327 and 1.372 μm, as indicated by the black dashed lines and marked as "Mode1" and "Mode2" in (a). The purple circles in the cavity center indicate the locations of the metal contact. Copyright (2012) The Japan Society of Applied Physics.

As an example, the field distributions of the two modes at 1.327 and 1.372 μm, as indicated by the black dashed lines and marked as "Mode1" and "Mode2," are shown in Figure 11.21c. The mode profile of the longer wavelength is more concentrated in the cavity center where the metal contact locates. We believe this is the reason why the intensity of the corresponding peak reduces so much in the EL spectrum compared with that in the PL spectrum.

By using the vertical PIN diode structure, enhanced resonant EL can be excited and demonstrated. However, due to the large cavity size and large effects of the electrical structures on the optical performances of the PhC cavities, the emission spectrum is rather poor, especially, the mode number is very large and the Q-factors are rather low. It is thus highly desirable to develop optimized electrical structures, which are compatible with PhC cavities with small size, can efficiently confine the injected carriers into the cavity and cause little modification to the cavity.

11.5.1.2 Lateral PIN Structure

Lateral PIN diode is just the configuration that can provide an excellent electrical injection solution for PhC nanocavities [46–50]. Figure 11.22 shows the 3D schematic diagram of the PhC nanocavity LED integrated with a lateral PIN diode, together with the cross-section of the cavity area. The heavily doped P+ and N+ regions are located laterally on the PhC slab, while the cavity region is left intrinsic. The metal contacts and electrodes are made far away from the PhC pattern regions.

The lateral PIN diode was fabricated by selective BF_2 and As ions implantation before patterning PhC cavity. In order to realize uniform doping concentration along the depth direction and high surface concentration simultaneously, ion implantation with multiple energies and doses was performed. The maximum p- and n-type doping concentrations are estimated to be about 8×10^{19} and 1.0×10^{20} cm^{-3}, respectively. The width of the intrinsic region of the PIN junction is designed to be 900 nm in the doping layout, and shrunk to about 860 nm due to the lateral diffusion after activation anneal. Figure 11.23 shows the SEM image of the fabricated device, together with the zoomed area of the PhC cavity, which is a common L3-type, with designed lattice constant of $a = 420$ nm and hole radius of $r = 0.24a$.

The I–V curve of the fabricated LED is shown in Figure 11.24, indicating a typical diode characteristic with a reverse leakage current about 18 μA for bias of −5 V. Figure 11.25a shows the EL spectra of the device under different injected

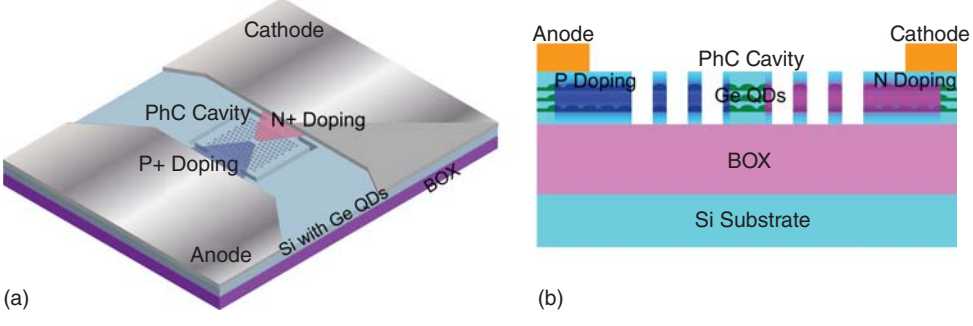


Figure 11.22 (a) Three-dimensional schematic diagram and (b) cross-section of the lateral PIN current-injected PhC cavity LED. Repinted from [46] with permissions from the OSA.

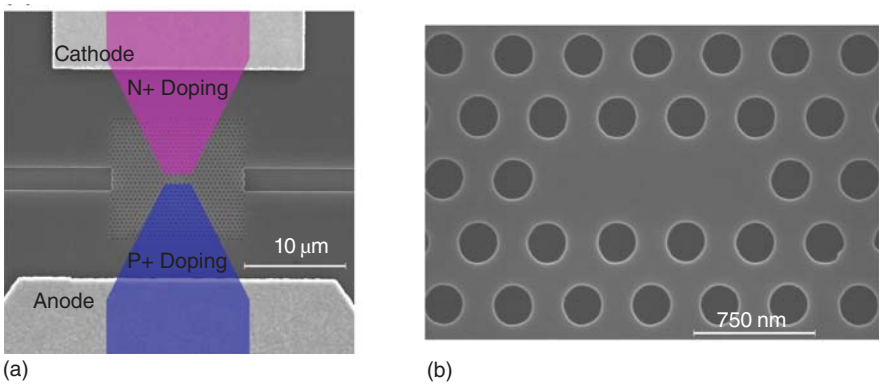


Figure 11.23 (a) SEM image of a fabricated lateral PIN current-injected PhC nanocavity LED, together with (b) the zoomed area of the L3-type PhC nanocavity. Repinted from [46] with permissions from the OSA.

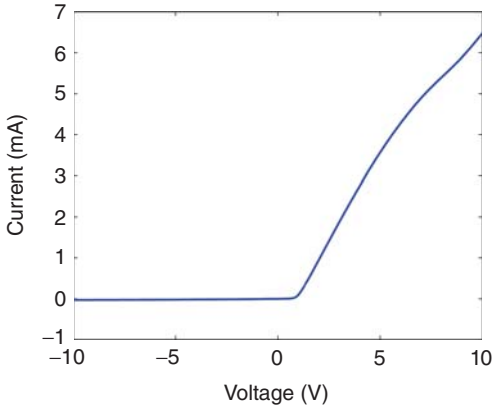


Figure 11.24 I–V curve of the fabricated LED. Repinted from [46] with permissions from the OSA.

currents. As the current becomes larger than 0.5 mA, clear resonant peaks appear in the spectrum. The simulated peak positions of PhC cavity modes are also shown on the top panel of Figure 11.25a. The Q-factor of the strongest peak in the EL spectrum (at 0.5 mA), corresponding to the fourth-order cavity mode, is about 260, according to Lorentz fitting shown in Figure 11.25b. It is similar with that (~265) of a reference cavity without electrical structure measured by PL, indicating that the heavily doped regions have few effects on the cavity. On the other hand, this Q-factor is lower than that (~400) of our previous PL results from a similar cavity with free-standing structure. It is mainly due to the weak optical confinement of BOX side and in-plane TE–TM coupling loss due to the vertical asymmetry. Moreover, compared with the simulation Q-factor (~530) of the corresponding structure, it is reduced by a factor of 2, which might be attributed to the scattering loss induced by fabrication roughness and the

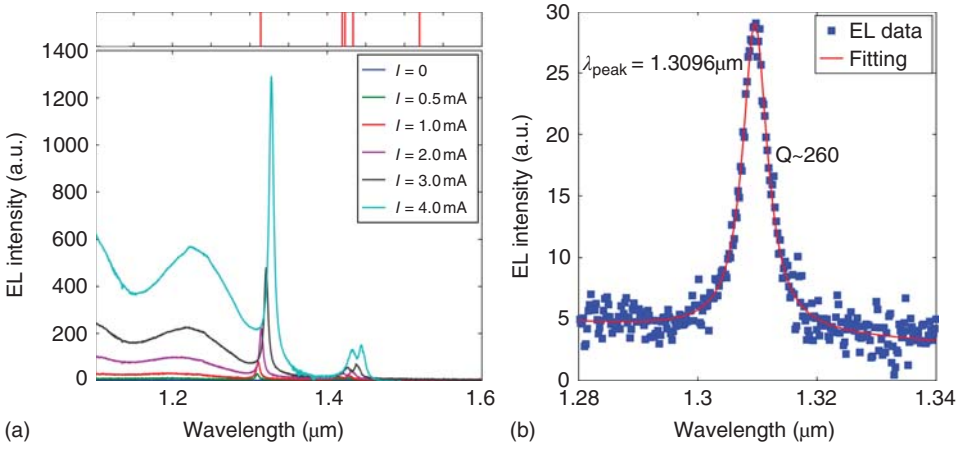


Figure 11.25 (a) EL spectra of the LED under different injected currents. The top panel shows the calculated peak positions of the PhC cavity modes. (b) Lorentz fitting of the strongest peak in the EL spectrum under 0.5 mA injected current. Repinted from [46] with permissions from the OSA.

absorption induced by the injected free-carriers. As the current increases, a broad peak around 1.22 μm appears in the spectra. This peak is caused by the enhanced emission from the PhC area around the cavity, because part of the current passes through the surrounding PhC area.

As the injected current increases, the peak wavelengths are red-shifted and Q-factors decrease, similarly to those of PL results. The mode intensity of the fourth-order cavity mode, which is obtained by integrating the resonant peak after subtracting the broad background, increases super-linearly against injected current, as shown in Figure 11.26. It is also similar to our previous PL and EL

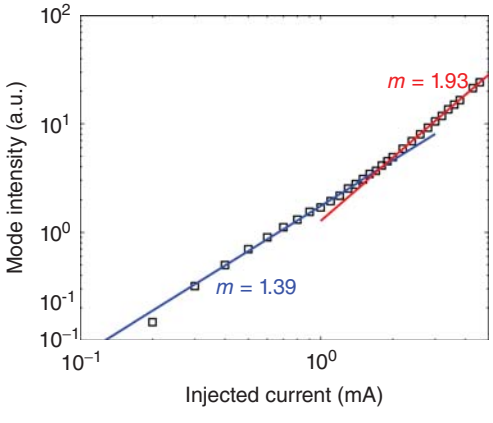


Figure 11.26 The relationship between the mode intensity of the fourth-order cavity mode and the injected current. Repinted from [46] with permissions from the OSA.

results. The dependence is usually empirically characterized by a nonlinear function $L \propto I^m$, where L is the mode intensity and I is the current. Interestingly, it is seen that at low injection level (<1.6 mA), the extracted nonlinear exponent m is 1.39 and increases to 1.93 at high injection level (>1.6 mA). One of the possible explanations for this increased nonlinearity is the increased 3D carrier localization inside the cavity at high injected current. Owing to the existence of the BOX layer and surrounding air holes, the diffusion of the carriers is partially blocked outward from the cavity. The carrier concentrations in the cavity might increase nonlinearly with the current. At high current density, strong band bending will also occur around the Ge/Si heterostructure. The overlap between electron and hole wave functions will be, therefore, enhanced and then the forbidden rules will be relaxed further. Moreover, as the resonant peak shifts toward longer wavelength, the emitter-cavity detuning decreases and more Ge QDs can be coupled to the cavity mode, which also contributes to the enhancement of the emission. The increased emission efficiency at high current is thought to be a result of the combination effects of these factors. However, more detailed studies are necessary to clarify which factors dominate the dependence.

Lateral PIN diode is thus demonstrated to be an effective current-injection structure to build LEDs. However, there is much space to improve the device performances. For example, the current at which the resonant peaks start to appear is still too high, mainly because a large part of current does not pass through the cavity. And the Q-factor of the cavity is still low.

11.5.1.3 Optimized Lateral PIN Structure

In order to improve the device performances, the device structures and fabrication processes of the lateral PIN PhC nanocavity LED are optimized, including the following improvements: (i) The P+ and N+ doping concentrations are reduced to 4×10^{19} cm^{-3} and the intrinsic width is increased to 1.2 μm in order to reduce the effect of heavily doped areas to the cavity. (ii) Isolation trenches are fabricated around the PhC patterns and heavily doped areas so that current can only pass through the PhC regions. (iii) Modified L3-type cavity is used, in which the holes at each edge of the cavity along the Γ-K direction are shifted and their radii are reduced. (iv) SiO_2 is deposited on top of the cavity to keep the cavity symmetric in vertical direction [51].

After these optimizations, strong resonant peaks can be also clearly observed in the EL spectrum, as shown in Figure 11.27a. The onset of the resonant peak occurs at the current of about 50 μA, which is almost one order lower than the above results. The optimized electrical structure, especially the isolation trenches, is attributed to this reduction because most of the carriers are efficiently injected into the cavity with very little loss. The Q-factor of the main resonant peak at 1.335 μm wavelength also increases to about 831. Compared to that of a reference diode without cavity, the emission intensity at the resonant wavelength is increased by a factor of 40 under 1 mA injected current, directly verifying the emission enhancement of the cavity.

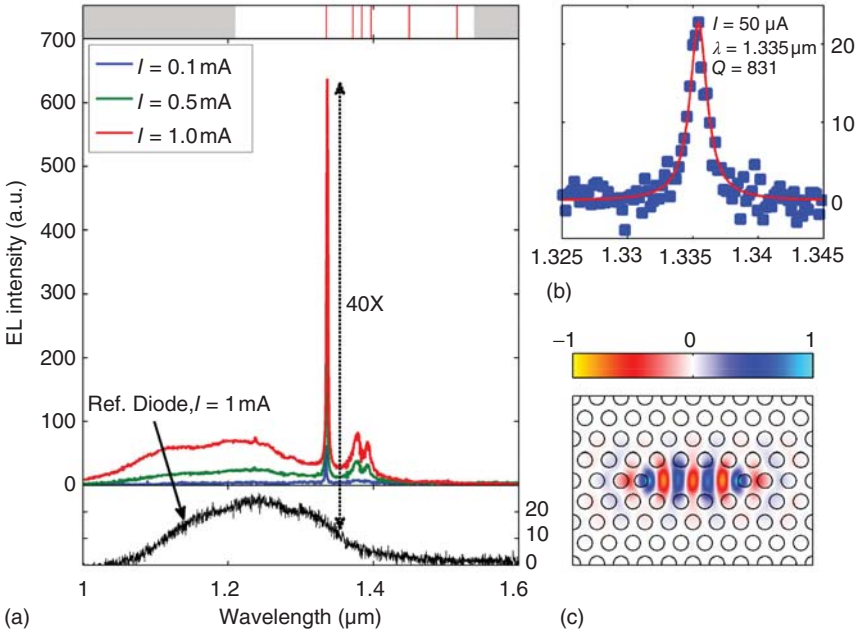


Figure 11.27 (a) EL spectra of the PhC nanocavity LED and the corresponding reference diode. The top panel shows the simulation results, in which the shading areas indicate the photonic band of the PhC, and the red lines indicate the cavity mode positions. (b) Lorentz fitting of the main resonant peak under 50 μA current. (c) Mode profile of the majority electrical field component of the fifth-order cavity mode. Copyright (2012) The Japan Society of Applied Physics.

The FDTD simulation results are shown in the top panel of Figure 11.27a. The main peak in the EL spectrum corresponds to the fifth-order cavity mode. The mode profile is shown in Figure 11.27c. The simulated Q-factor of this mode is about 774, which shows reasonable agreement with the experimental result. The second- and third-order modes are also seen as the broader peaks in the EL spectrum. However, we could not observe the resonant peaks corresponding to the fundamental and first-order modes. This is because there are very few Ge QDs spectrally coupled to these two lower-order modes. Owing to the high-temperature fabrication processes, there is strong Si/Ge inter-diffusion [52]. The emission peak of the Ge QDs is largely blue-shifted from 1.5 to 1.25 μm, and the intensity is also significantly reduced in the wavelength range where the fundamental and first-order modes are located, as one can see in the PL spectra from the unpatterned region of the sample before and after device fabrication in Figure 11.28. A further investigation shows that the high-temperature rapid thermal annealing (RTA) for ions activation is the main factor to be blamed. By optimizing the RTA condition to reduce the Si/Ge intermixing, we are able to not only shift the resonant wavelength of the LEDs to the popular 1.5 μm range, but also increase the light emission intensity further.

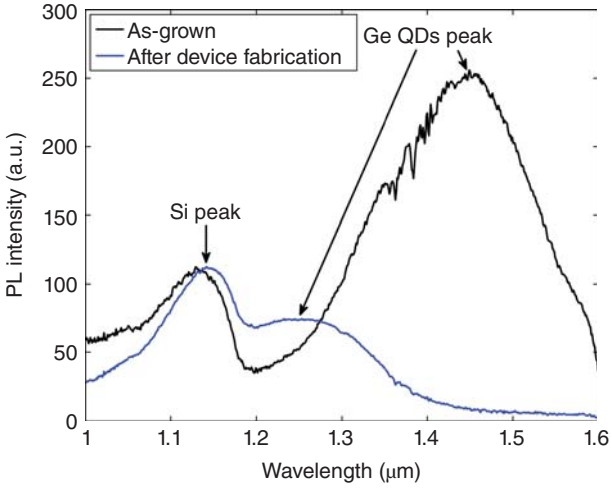


Figure 11.28 PL spectra from the unpatterned regions of the sample before and after device fabrication. During the PL recording, the grating used in the monochromator and objective lens used in the confocal microscope were changed in order to obtain the highest PL signal intensity, at the cost of the spectrum resolution. Copyright (2012) The Japan Society of Applied Physics.

Both the mode intensity of the main peak and integrated EL intensity over the full wavelength range are plotted against the current in Figure 11.29. Compared with those of the reference diode, both the absolute intensity and slope of the integrated EL intensity versus current (which can be considered as a measure of the external quantum efficiency of the LED) are enhanced. On the other hand, the mode intensity of the main peak first increases against the current, and then saturates and even decreases at higher current levels. Moreover, as for the evolution of the EL with the current, we found that although the resonant peak did not increase at higher current levels, the broad background kept increasing. These suggest that the light emission from Ge QDs is less coupled to the cavity mode, but to the broad background in the EL spectrum. As this background signal comes from the surrounding PhC hole regions, we can conclude that at a high injection level, the injected carriers are not only confined in the cavity, but also partially diffused to the surrounding PhC hole regions.

The absolute output power of the LED was also measured with a single-mode fiber positioned on top of the cavity. The measured power under different currents is shown in the inset of Figure 11.29. We can clearly see that there is a measurable output when the current is injected into the device. The output power reaches 6 pW at 3 mA current. Although it is still very low, this result indeed verifies the potential in the practical application of the device. To increase the output power further, we may increase the layer number of Ge QDs, optimize the fabrication process as mentioned above, and increase the collection efficiency by using a multimode fiber.

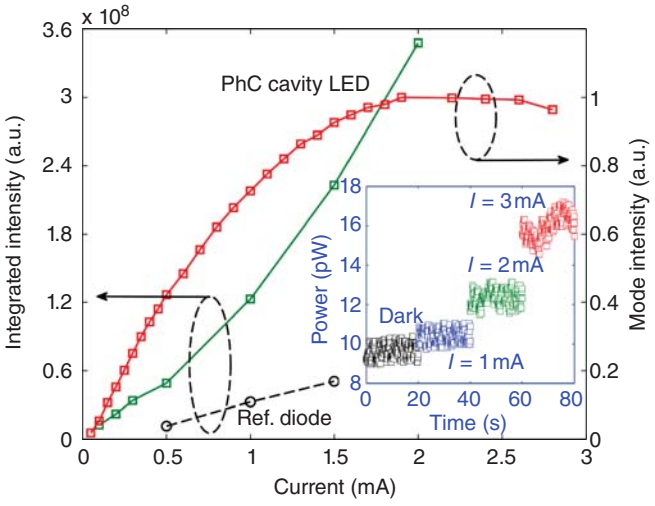
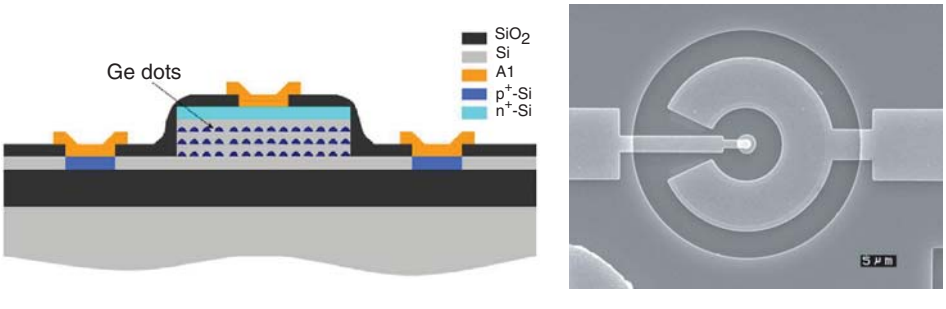


Figure 11.29 Mode intensity of the main peak and integrated EL intensity of the PhC nanocavity LED and reference diode over the full wavelength range under different currents. The inset shows the output power of the LED collected by a single-mode fiber and measured using a powermeter. The dark power means the power value measured in the powermeter without current injection. Copyright (2012) The Japan Society of Applied Physics.

11.5.2 Microdisk

For microdisk, there are not so many choices for the electrical structure [53]. A vertical PIN diode should be the most natural and easiest way. Figure 11.30a shows the schematic structure of the microdisk LED with a vertical PIN diode. For microdisk, the total thickness of Si/Ge active layer is not critical. In order to



(a) (b)

Figure 11.30 (a) Cross-section view of the structure of the microdisk LED. (b) SEM image of a fabricated microdisk LED with diameter of 2.8 μm. Repinted from [53] with permissions from the OSA.

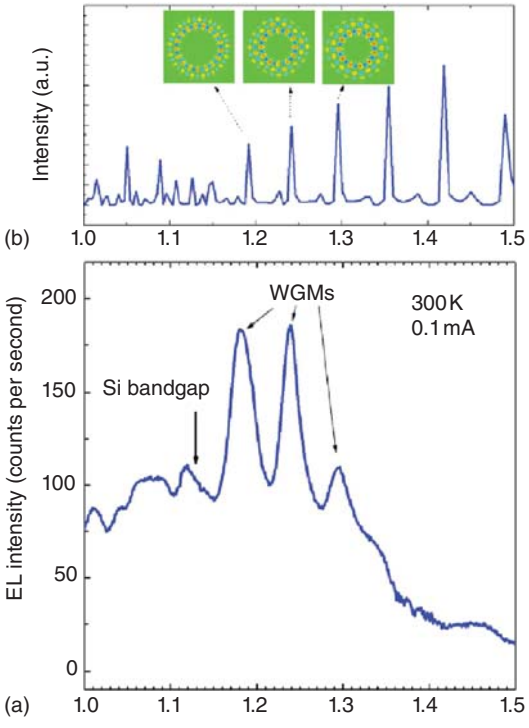


Figure 11.31 (a) EL spectrum of the microdisk LED under current of 0.1 mA recorded at room-temperature. (b) Calculated wavelengths of TM-like WGMs supported by the microdisk. The insets show the mode profiles of three WGMs. Repinted from [53] with permissions from the OSA.

enhance the total number of Ge QDs in the devices, 10 layers of the Ge QDs were grown on SOI wafer with 260 nm-thick top Si layer. To fabricate the vertical PIN junction, As ions were implanted into the top Si for the N+ layer. A 160-nm-thick p-type Si film was retained to work as the current pathway and was selectively implanted by BF_2 ions to form the P + area. The SEM image of a fabricated LED with diameter of 2.8 μm is shown in Figure 11.30b.

Figure 11.31a shows the EL spectrum under an injected current of 0.1 mA (~800 A cm^2). Clear EL is observed in the wavelength range of 1 – 1.4 μm. Several peaks are seen in the spectrum, and can be assigned to the optical resonance in the microdisk. There are three major peaks locating at 1.185, 1.238, and 1.295 μm, respectively. Figure 11.31b shows the calculated TM polarized-like resonant peaks of the device. Three peaks locating at 1.191, 1.241, and 1.296 μm are well corresponded to the three major peaks in the EL spectrum. The mode profiles of these peaks are shown by the insets in Figure 11.31b. They are WGMs with the order of $TM0_{2,27}$, $TM0_{3,12}$, and $TM0_{3,11}$. All these WGMs are TM-like polarized, and no clear TE-like modes are observed in the spectrum. Based on

calculation of the fundamental slab mode indexes in the 0.5-μm-thick disk and the 0.16-μm-thick surrounding slab, it is found that the difference of TM mode indexes in these two areas is larger than that of TE modes, suggesting that the energy loss of TM modes due to coupling to the surrounding slab is smaller than that of TE modes. This leads to the domination of the TM modes in the spectrum. The calculated Q-factor of these WGMs is in the range of 400–800 which is much smaller than calculated Q-factors (~4800) of a typical microdisk resonator with the surrounding area completely etched to the BOX. It is reasonable as the energy loss induced by the coupling to the remaining surrounding Si slab is much larger than that of a completely etched microdisk. The Q-factors of WGM peaks in the EL spectrum are in the range of 50–90 and they are smaller than the calculated value of 400–800. The reason for the decrease of quality factors is attributable to the absorption loss induced by the Al contact on the microdisk and free carrier absorption in the high doping layer. The scattering loss induced by the Al contact arm located on the top of the disk may also decrease the Q-factor. No obvious FP modes, which are induced by the reflection at the edges of the disk, are observed in the EL spectra. Because a 160-nm-thick Si layer remains as the current pathway in the surrounding area of the disk, the reflection at the edge is smaller than that of a fully etched microdisk resonator. It means that most of the optical power escapes from the disk when light is reflected at the edge, which makes the resonance weak and difficult to be observed.

The current dependence of the light emission from microdisk is very similar to that from PhC cavities, which will not be described here anymore. From the above results, the performance of microdisk LED, especially the Q-factor, suffers from the thick Si slab for electrical path, heavily doped region and metal contact on top of the microdisk. The future work to improve the performance includes reducing the slab thickness, and minimizing the overlap between WGMs and electrical structures. Moreover, because the radiation from the microdisk is mainly in the direction of the in-plane, a waveguide coupling structure should benefit the light extraction from the microdisk, thus increasing the emission intensity.

11.6 Conclusion

Room-temperature enhanced light emission from Ge QDs, both optical- and electrical-excited, is successfully demonstrated by embedding them into optical microcavities, including 2D PhC cavities and microdisks/rings. The light emission properties, such as emission wavelength, Q-factor, and emission intensity, are strongly dependent on the excitation conditions, device structures, and fabrication processes. Concerning the device performance, PhC cavities seem superior to microdisks/rings due to their higher Q-factor, smaller mode volume, and larger light extraction efficiency. These results show a promising way to realize Si-based light emitting devices for optical interconnection. However, there is still much work to do to make these devices closer to a practical level.

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12
Ge-on-Si Lasers

Jifeng Liu

12.1
Introduction

A monolithic laser source on Si has been considered a "holy-grail" since the substantial benefits of electronic–photonic integration was envisioned in the early 1990s [1, 2]. However, indirect band gap semiconductors such as Si and Ge are traditionally regarded unsuitable for laser diodes (LDs) due to their inefficient radiative recombination. To overcome this issue, extensive investigations have been conducted on porous Si [3], Si nanocrystals [4], ultrathin Si quantum wells (QWs) [5], Er doped Si [6] or Si nanostructures [7], SiGe nanostructures [8], GeSn [9], Si Raman lasers [10], and III–V lasers grown on [11] or bonded to Si [12]. While stimulated emission from ultrathin Si QWs has been observed, the gain is not enough to overcome the loss to enable lasing [13]. III–V semiconductors on Si have successfully demonstrated lasing under electrical pumping, yet it has its limitations for high-volume, large-scale electronic–photonic integration. Epitaxial growth of III–V semiconductors on Si typically requires a thick buffer layer, making complementary metal oxide semiconductor (CMOS) integration difficult. Hybrid integration of III–V lasers on Si by chip bonding has achieved significant progress in recent years; yet, scaling up to wafer-scale fabrication remains a challenge, partially due to the wafer size mismatch (i.e., 200 mm maximum for III–V wafers versus 300 and 450 mm for Si wafers) and partially due to the processing flow compatibility.

Since the late 1990s, Ge has become an interesting candidate for active photonic devices on Si due to its pseudo-direct gap behavior and compatibility with Si CMOS technology [14]. The band structure of bulk Ge is schematically shown in Figure 12.1a. Although conventionally Ge is considered an indirect gap semiconductor, the energy difference between its direct gap at the Γ valley and indirect gap at the L valleys is only 136 meV [16], or ~5 $k_B T$ at room temperature (k_B is the Boltzmann constant). Realizing this small energy difference between the direct and indirect gaps, it is natural to ask if one could enhance the direct gap emission simply by increasing the injection level such that some of the injected electrons spill into the direct Γ valley.

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Haynes first reported photoluminescence (PL) from the direct band gap transition of Ge at room temperature [17]. In 1963, Nobel Prize laureate Herbert Kroemer first proposed that lasing from the direct gap transition of Ge could be implemented by using heterojunction structures to inject carriers into the direct Γ valley [18]. In the 1960s, Haynes and Nilsson studied PL from the direct gap transition of Ge at room temperature and revealed that the radiative recombination rate of the direct transition in Ge is four to five orders of magnitude higher than that of the indirect transition [19]. In the 1970s, van Driel *et al.* [20] studied the direct gap PL of Ge at high injection levels. They suggested that population inversion has been observed at an optical pumping level of ~100 kW cm^{-2} because they derived a quasi-Fermi level separation that was 50 meV greater than the direct gap of Ge from the PL data. Klingenstein and Schweizer [21] further observed a significant optical bleaching of ~70% upon high power pulsed laser pumping of intrinsic bulk Ge crystal at low temperatures. In the 1980s, Wagner *et al.* studied low-temperature PL from heavily doped Ge. Doping levels higher than the solubility limit were achieved by ion implantation and laser annealing [22–24]. For n^+ bulk Ge, they have observed that the high energy edge of the PL spectra blue-shifted to shorter wavelengths with the increase of doping level due to band filling of the L valleys. More recently, room-temperature continuous wave (CW) pump-probe studies of intrinsic Ge-on-insulator (GeOI) showed up to 60% bleaching at photon energies greater than the direct band gap using a pumping photon energy of 0.84 eV [25]. However, no net optical gain has ever been reported from intrinsic Ge in the past 50 years.

The significant optical bleaching of direct gap absorption indicates that population inversion of direct gap transition indeed happens at high injection levels; yet the lack of net optical gain in intrinsic bulk Ge shows that the gain from direct gap transition cannot overcome loss mechanisms such as free carrier absorption (FCA). In the next section we will present a theoretical modeling showing why intrinsic bulk Ge cannot achieve net optical gain, and how to overcome this issue by introducing tensile strain and n-type doping for band-engineering.

12.2 Modeling and Analyses of Band-Engineered Ge Optical Gain Media

12.2.1 Optical Gain from the Direct Gap Transition of Ge

12.2.1.1 Unstrained Ge

The net optical gain of Ge upon carrier injection equals to direct gap optical gain subtracted by FCA losses [15, 26, 27]. We stress that, in this chapter, FCA refers to *any* optical losses related to the free carriers (doped and injected), including both intraband and interband transitions. It is not restricted to intraband transitions following the Drude model. The gain coefficient of the direct band transition at a given photon energy, $\gamma_\Gamma(h\nu)$, is related to the absorption coefficient of the direct

band transition, $\alpha_\Gamma(h\nu)$, by

$$\gamma_\Gamma(h\nu) = |\alpha_\Gamma(h\nu)|(f_c - f_v), \tag{12.1}$$

where $(f_c - f_v)$ is the well-known population inversion factor for direct band transitions at the photon energy of $h\nu$ [28]. For bulk Ge the direct band-to-band absorption can be expressed as

$$|\alpha_\Gamma(h\nu)| = \frac{A\left(\sqrt{h\nu - E_g^\Gamma}\right)}{h\nu}, \tag{12.2}$$

where $h\nu$ is the photon energy, $E_g^\Gamma = 0.8$ eV is the direct gap of bulk Ge, and A is a constant related to the transition matrix element and the effective mass of the material. Fitting to the experimentally measured absorption spectrum yields $A = 1.9 \times 10^4\,\mathrm{eV}^{1/2}\,\mathrm{cm}^{-1}$ for bulk Ge.

12.2.1.2 Tensile Strained Ge

The energy difference between the direct and indirect gaps of Ge can be further reduced by tensile strain, as schematically shown in Figure 12.1b. With biaxial tensile stress, both direct and indirect gaps shrink, but the direct gap shrinks faster. Therefore, Ge transforms from an indirect gap material toward a direct gap material with the increase of tensile strain. Moreover, the top of the valence band is determined by the light hole band under biaxial tensile stress. The small effective mass of the light hole band reduces the density of states in the valence band, which in turn decreases the threshold for optical transparency and lasing.

As the valence band becomes non-degenerate at $k = 0$ for tensile-strained Ge, Eq. (12.2) is modified to fit the absorption spectra of tensile-strained Ge:

$$|\alpha_\Gamma(h\nu)| = \frac{A\left(0.318\sqrt{h\nu - E_g^\Gamma(lh)} + 0.682\sqrt{h\nu - E_g^\Gamma(hh)}\right)}{h\nu}, \tag{12.3}$$

where $E_g^\Gamma(lh)$ and $E_g^\Gamma(hh)$ are the direct band gaps associated with the light and heavy hole bands, respectively, and the factors of 0.318 and 0.682 are the relative contribution of light and heavy hole bands to the total absorption based on the ratio of their reduced effective mass. Fitting to the experimentally measured absorption spectrum of 0.25% tensile-strained Ge yields $A = 2.0 \times 10^4\,\mathrm{eV}^{1/2}\,\mathrm{cm}^{-1}$, similar to that of the bulk Ge. The dependence of $E_g^\Gamma(lh)$ and $E_g^\Gamma(hh)$ on in-plane tensile strain $\varepsilon_{||}$ under biaxial stress state in a [001] oriented Ge thin film can be derived using the deformation potential theory [29, 30]:

$$\begin{aligned} E_g^\Gamma(lh) = E_g^\Gamma(0) + a(\varepsilon_\perp + 2\varepsilon_{||}) + \Delta_0/2 - 1/4\,\delta E_{100} \\ -1/2\sqrt{\Delta_0^2 + \Delta_0\delta E_{100} + 9/4\ (\delta E_{100})^2} \end{aligned} \tag{12.4a}$$

$$E_g^\Gamma(hh) = E_g^\Gamma(0) + a(\varepsilon_\perp + 2\varepsilon_{||}) + 1/2\delta E_{100}, \tag{12.4b}$$

where $E_g^\Gamma(0) = 0.8005 \pm 0.0007$ eV is the direct bandgap of unstrained bulk Ge at room temperature; $a = 8.97 \pm 0.16$ eV and $b = -1.88 \pm 0.12$ eV are deformation potential constants of [100] Ge at room temperature; $\varepsilon_\perp = -\varepsilon_{||}/1.33$ is

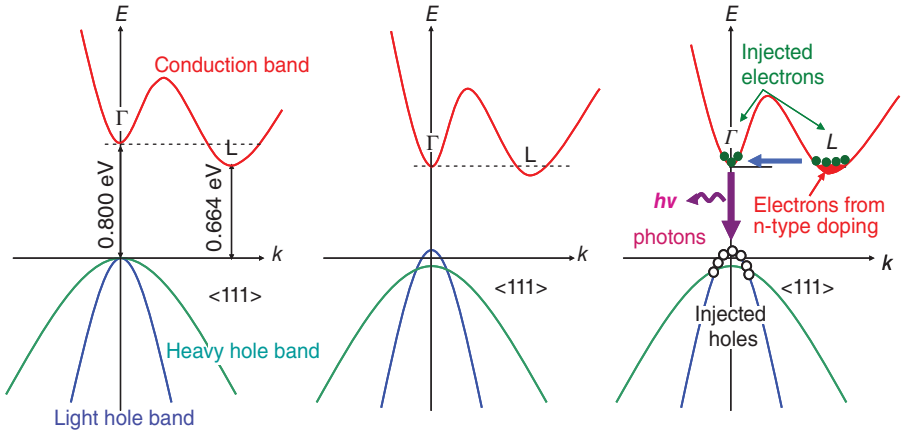

Figure 12.1 (a) Schematic band structure of bulk Ge, showing a 136 meV difference between the direct gap and the indirect gap, (b) the difference between the direct and the indirect gaps can be decreased by tensile strain, and (c) the rest of the difference between direct and indirect gaps in tensile-strained Ge can be compensated by filling electrons into the L valleys via n-type doping. Because the energy states below the direct Γ valley in the conduction band are fully occupied by extrinsic electrons from n-type doping, injected electrons are forced into the direct Γ valley and recombine with holes, resulting in efficient direct gap light emission. Reprinted from [15] under the Author's Copyright Transfer Agreement with the Optical Society of America (OSA).

the strain perpendicular to the Ge film; $\delta E_{100} = 2b(\varepsilon_{\perp} - \varepsilon_{||})$; and $\Delta_0 = 0.289$ eV is the energy of spin-orbital splitting in Ge. In calculating the gain coefficients for tensile-strained Ge using Eq. (12.1), one also needs to note that the population inversion factors $(f_c - f_v)$ are different for *lh* and *hh* transitions, respectively, because the same emitted photon energy corresponds to different k vectors in the lh and hh bands for the direct gap transition. One needs to calculate these population inversion factors separately and then sum them up:

$$\gamma_{\Gamma}(h\nu) = |\alpha_{\Gamma,lh}(h\nu)|\left(f_c - f_v\right)_{lh} + |\alpha_{\Gamma,hh}(h\nu)|\left(f_c - f_v\right)_{hh} \tag{12.5}$$

12.2.2

Band-Engineering by Combining Tensile Strain with N-type Doping

Theoretically, Ge can be transformed into a direct gap material with ~2% biaxial or ~4.5% uniaxial tensile strain along the <100> direction [15, 26, 31–33]. However, such a large tensile strain is difficult to achieve, as will be discussed in detail in Section 12.3. In addition, the band gap decreases to ~0.5 eV at ~2% biaxial tensile strain and the corresponding emission wavelength shifts to 2500 nm in that case. To obtain optical gain from the direct gap transition of Ge while maintaining the emission wavelength around 1550 nm, n-type doping has been combined with 0.2–0.3% tensile strain in order to compensate the energy difference between

direct and indirect gaps (Figure 12.1c) [15]. Liu *et al.* [15] showed that the n-type doping level needed decreases from for 10^{20} cm^{-3} to 7×10^{19} cm^{-3}, when tensile strain increases from 0 to 0.25%. For even larger tensile strain the required n-doping level can be further reduced as the energy difference between direct and indirect gaps becomes smaller. As the lower energy states in indirect L valleys are already occupied by electrons from n-type doping, upon carrier injection some injected electrons are forced to occupy the direct Γ valley and recombine with holes radiatively by means of efficient direct transitions. Furthermore, because the radiative recombination rate of the direct transition is four to five orders of magnitude higher than that of the indirect transitions [19], the injected electrons in the Γ valley are depleted much faster than those in the L valleys. In order to maintain the quasi-equilibrium of electrons in the conduction band, the electrons initially injected into the L valleys will populate the Γ valley following inter-valley scattering, as shown by the horizontal dashed arrow in Figure 12.1c. This process results in further radiative recombination through efficient direct transitions. Liu *et al.* [15] show that the optical gain and stimulated emission from the direct gap transition of Ge can be achieved.

Aldaghri *et al.* [33] further analyzed the effect of crystallographic orientation of Ge thin films and QWs on the tensile strain and n-type doping needed to compensate the energy difference between the direct and indirect band gaps. It was found that for tensile strain engineering alone [100] Ge is the best choice, where 1.7% biaxial tensile strain or 4.6% uniaxial tensile strain can transform Ge into a direct gap semiconductor. On the other hand, for moderately tensile-strained Ge that requires n-type doping to compensate for the rest of the energy difference between direct and indirect gaps, [111] Ge could be a better choice. This applies to bulk Ge with <0.8% biaxial tensile strain, as well as Ge QWs with <1.4% biaxial tensile strain or <2% uniaxial strain. A technical challenge, though, is that the growth of [111] Ge is not directly compatible with regular Si substrates used in CMOS.

12.2.3 FCA Losses

With the band-engineering approach and optical gain modeling discussed above, now the critical question is: can optical gain from the direct gap transition overcome the FCA losses from the n-type doping and the injected carriers?

Empirically, the FCA coefficient in bulk Ge can be expressed as a summation of free electron absorption (FEA) and free hole absorption (FHA) [15, 27, 34, 35]:

$$\alpha_f(\lambda) = 3.4 \times 10^{-25} N\lambda^{2.25} + 3.2 \times 10^{-25} P\lambda^{2.43}, \tag{12.6a}$$

where $\alpha_f(\lambda)$ is the FCA coefficient in unit of cm^{-1}, N and P are respectively electron and hole concentration in unit of cm^{-3}, and λ is the wavelength in unit of nm. This empirical equation is an extrapolation from the Drude model using the FCA data measured at $\lambda > 2000$ nm for bulk Ge (i.e., single crystal wafer without strain). Recent studies on FEA in −0.07% *compressively* strained n$^+$ Ge (n−1×10^{19} cm^{-3})

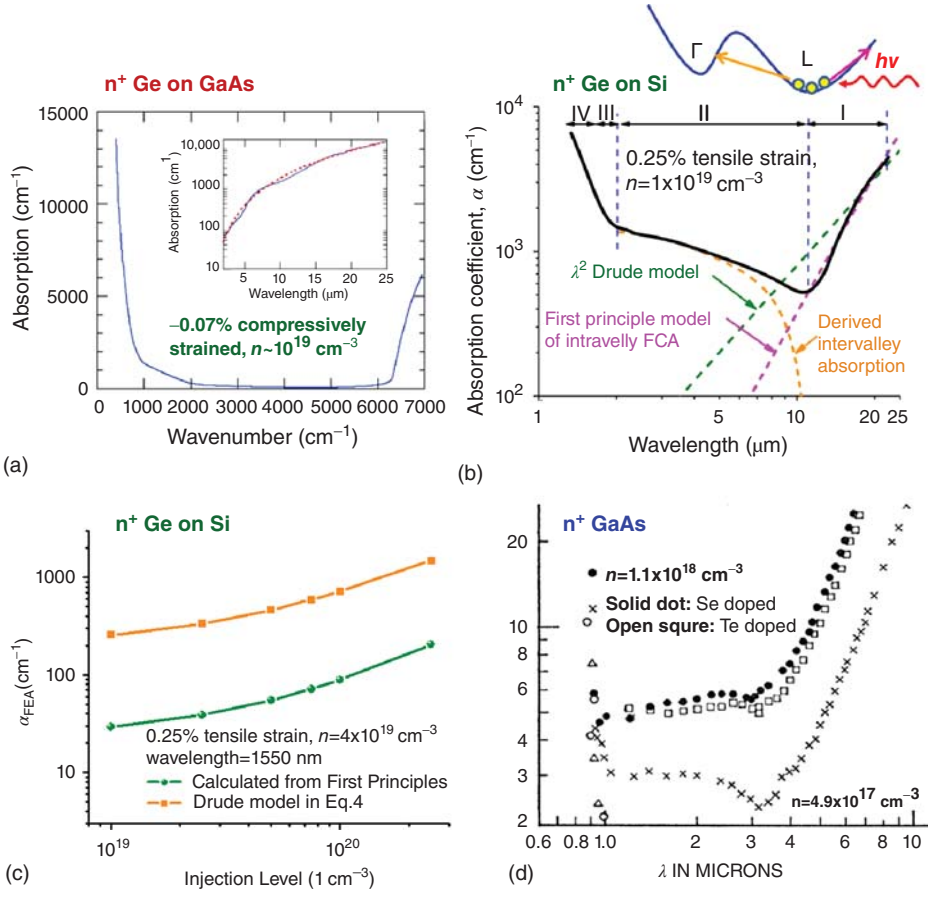

Figure 12.2 Free carrier absorption (FCA) in n^+ Ge. (a) −0.07% compressively strained n^+ Ge on GaAs $n = 10^{19}$ cm^{-3}. Repinted from [36] with permissions from the OSA. (b) 0.25% tensile-strained n^+ Ge on Si, $n = 1 \times 10^{19}$ cm^{-3}. The inset schematically shows intra-L-valley FCA and intervalley scattering absorption (IVSA) from the L to the Γ valley. Regions I–IV are dominated by intra-L-valley FCA, L-to-Γ IVSA, indirect gap absorption, and direct gap absorption, respectively. Reprinted from [37] under the Author's Copyright Transfer Agreement with the OSA. (c) Free electron absorption α_{FEA} versus injection level at $\lambda = 1550$ nm from the first principle model compared to the Drude model. (d) Comparison to FCA in n-GaAs, which also demonstrates IVSA except that in this case the direction is from Γ to L valleys, opposite to Ge. Reprinted from Ref. [38] with permissions from American Physical Society (APS).

grown on GaAs substrates suggests that the prefactor of the FEA in Eq. (12.6a) is overestimated by a factor of 2, while the proportional relation to $\lambda^{2.25}$ resembling Drude model still holds ([36], Figure 12.2a). So, in this case, the Eq. (12.6a) is corrected as:

$$\alpha_f(\lambda) = 1.7 \times 10^{-25} N\lambda^{2.25} + 3.2 \times 10^{-25} P\lambda^{2.43} \tag{12.6b}$$

Note that in both Eqs (12.6a) and (12.6b) the FHA is much greater than FEA: a factor of 4× according to Eq. (12.6a), and a factor of 8× according to Eq. (12.6b). Therefore, FHA is the dominant factor in Ge FCA losses. As will be discussed in Section 12.2.4, the major reason that prevents intrinsic Ge from achieving net optical gain is the high injected-carrier density required for population inversion and the associated FHA losses. On the other hand, because the Fermi level of electron is already approaching the Γ valley in n^+ Ge, the required injected carrier density for population inversion is much smaller. Thus, the FHA is greatly reduced and net optical gain can be achieved.

Remarkably, it has been recently demonstrated that the Drude model actually fails to describe the FCA in *tensile-strained* n^+ Ge-on-Si [37, 39]. As shown in Figure 12.2b, the Drude model significantly deviates from the experimental data at $\lambda < 15\,\mu m$ with an overestimated FCA. This overestimate is fundamentally due to the fact that the Drude model does not consider the band structure of Ge at all. In reality, to implement intra-L-valley absorption of photons with an energy $\gg 0.1$ eV, significant momentum transfer from phonon scattering is needed (see the inset of Figure 12.2b). The larger the photon energy, the larger the momentum mismatch to implement the intravalley absorption. Therefore, a Drude model shows an increasingly bigger deviation from the experimental data at shorter wavelengths. A first-principle model taking into account the band structure of Ge as well as acoustic phonon, optical phonon, and impurity scattering is much more consistent with the experimental results [37]. Figure 12.2c further shows the FEA as a function of injected carrier density calculated by the first principle model versus Drude model for 0.25% tensile-strained Ge with an n-doping level of $4 \times 10^{19}\,cm^{-3}$. The FEA from the Drude model is approximately eight times larger than the first principle model for intra-L-valley absorption.

Another important feature in the FEA of tensile-strained Ge is that the absorption starts to increase again at $\lambda < 11\,\mu m$. This phenomenon cannot be explained by the Drude model at all. We attribute it to the onset of intervalley scattering absorption (IVSA) from the indirect L valleys to the direct Γ valley. This conclusion is based on the fact that the observed absorption edges in Regime II for tensile-strained Ge samples with different n-type doping levels are consistent with the energy difference between the Γ valley and the Fermi level [37]. The shape of the FEA absorption curve is also remarkably similar to that of n^+ GaAs [38], where IVSA at shorter wavelengths had been clearly observed (Figure 12.2d). Note that the IVSA process in n^+ Ge promotes electrons from the indirect L valleys to the direct Γ valley, which in turn enhances light emission and optical gain from the direct gap transition of Ge. This process is exactly opposite to the case of III–V semiconductors, where the intervalley absorption from the direct Γ valley to the indirect L valleys is detrimental to the optical gain and lasing. It is also interesting to note that IVSA has not been observed in previous literature on bulk n^+ Ge (0 strain) or −0.07% compressively strained n^+ Ge grown on GaAs reported recently [36]. Therefore, the 0.25% tensile strain in the n^+ Ge films seems to enhance IVSA by decreasing the energy difference between L and Γ valleys and making more initial and final states accessible to phonon-assisted IVSA. Indeed,

pressure-dependent *ab initio* calculation shows that the contributions of various phonons to the intervalley scattering are quite dependent on the energy separation between conduction band valleys [40].

12.2.4
Band Gap Narrowing in n^+ Ge

While the effect of tensile strain on the band gap of Ge is well understood using the deformation potential theory (Section 12.2.1), the effect of n-type doping appears more complicated. For *insitu* doped n^+ Ge grown at 650 °C, there is no significant shift in PL peak position up to an n-type doping level of $1\times10^{19}\,\mathrm{cm}^{-3}$ (Figure 12.3a, [44]). This result is consistent with the electroreflectance data reported by Lukeš and Humličeк [45] showing no significant change in direct band gap for an n-type doping level up to $2\times10^{19}\,\mathrm{cm}^{-3}$. A possible reason for such a behavior is that the effective density of states in the conduction band of Ge is $N_c = 5\times10^{18}\,\mathrm{cm}^{-3}$ at room temperature, meaning that a doping level of $\sim10^{19}\,\mathrm{cm}^{-3}$ is needed to transform it into a degenerate semiconductor and induce appreciable BGN (band gap narrowing). On the other hand, for Ge with $n > 2\times10^{19}\,\mathrm{cm}^{-3}$ achieved either by drive-in diffusion from delta doped Ge/P stacks [41, 46] or by low temperature molecular beam epitaxy (MBE, [47]), the emission peak starts to show a red-shift with the increase of doping level (Figure 12.3b). By analyzing the PL peak position versus doping levels, Camacho-Aguilera *et al.* [41] have found that the direct BGN at $2\times10^{19}\,\mathrm{cm}^{-3} < n < 5\times10^{19}\,\mathrm{cm}^{-3}$ can be expressed as a simple linear relation (Figure 12.3b):

$$E_g^{\Gamma}(n) = E_g^{\Gamma}(n=0) - 0.013 - 10^{-21}n, \tag{12.7}$$

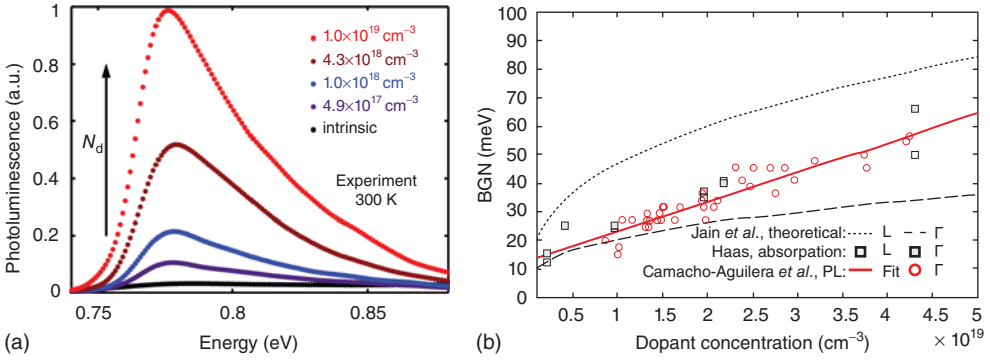

Figure 12.3 Band gap narrowing (BGN) in n-Ge. (a) PL spectra of 0.25% tensile- strained Ge on Si, showing no significant BGN up to $n = 1\times10^{19}\,\mathrm{cm}^{-3}$ for *in situ* doped Ge. (b) BGN versus n-doping reported by [41]. (Derived from experimental PL data.) [42]. (Derived from experimental absorption spectra.) [43]. (From theoretical modeling.) Reprinted from [41, 44] with permissions from AIP Publishing, LLC.

where $E_g^{\Gamma}(n)$ and $E_g^{\Gamma}(n=0)$ are the direct band gaps with and without doping, respectively, in unit of eV and n is the doping level in unit of cm^{-3}. Equation (12.7) seems to slightly overestimate the BGN for $n > 5 \times 10^{19}\,cm^{-3}$, though. For example, Eq. (12.7) predicts a direct band gap of 0.69 eV for relaxed Ge with $n = 10^{20}\,cm^{-3}$, while the PL data indicate a direct band gap of ~0.72 eV for $10^{20}\,cm^{-3}$ Sb-doped Ge grown by MBE [47]. The amount of BGN given by Eq. (12.7) is generally smaller than previous experimental reports based on optical absorption spectra [42] and the theoretical prediction proposed by Jain and Roulston [43]. It is possible that in Hass *et al.* defect-induced band tails lead to an overestimate of the red-shift from the absorption spectra.

12.2.5
Net Optical Gain Analyses for Tensile-Strained N^+ Ge

Using Eqs (12.1) – (12.7), we can calculate the net gain from Ge upon carrier injection, which is the difference between the direct gap optical gain and the FCA loss. Figure 12.4a shows the net gain a function of injected carrier density for unstrained and tensile-strained Ge with and without n-type doping [26]. In this figure, FCA was calculated using Eq. (12.6a), and no BGN had been considered. Because tensile-strained and unstrained Ge have different band gaps, in order to compare the optical gain for each case we choose photon energies corresponding to the peak of each optical gain spectrum at an injected carrier density of $1 \times 10^{19}\,cm^{-3}$. The theoretical modeling shows that unstrained intrinsic Ge initially exhibits significant optical bleaching upon carrier injection; yet, at an injection level of $\Delta n > 4 \times 10^{18}\,cm^{-3}$ the absorption starts to increase again because the optical gain can no longer catch up with FCA losses. The lowest loss achievable is $\sim 100\,cm^{-1}$ at $\Delta n = 3.5 \times 10^{18}\,cm^{-3}$ for unstrained intrinsic Ge. Even considering reduced FEA in Eq. (12.6b) or the first principle model of tensile-strained n-Ge, net gain is still impossible for unstrained intrinsic Ge because the FCA is dominated by FHA in any case. As a result, we can observe only optical bleaching in unstrained intrinsic Ge but not optical gain. This prediction is in good agreement with previous experimental results [21, 25]. On the other hand, in n^+ Ge with an n-type doping level of $7 \times 10^{19}\ cm^{-3}$, net gain can be obtained at injected carrier densities above $10^{18}\,cm^{-3}$ even without tensile strain. A major difference from the intrinsic Ge case is that the Fermi level is already raised close to the Γ valley by n-type doping (Figure 12.1c) so that a much smaller amount of injected carriers is needed to achieve population inversion. As a result, FHA is significantly reduced and net gain is enabled. The modeling also shows that the net gain of n^+ Ge can be improved by greater than five times from less than 100 to greater than $500\,cm^{-1}$ by introducing 0.25% tensile strain due to a smaller energy difference between Γ and L valleys.

Figure 12.4b further shows a refined calculation of net optical gain for 0.25% tensile strain Ge with $n = 4.5 \times 10^{19}\,cm^{-3}$ at $\lambda = 1700$, 1650, 1600, and 1550 nm as a function of injected carrier density, using the first principle model of FEA

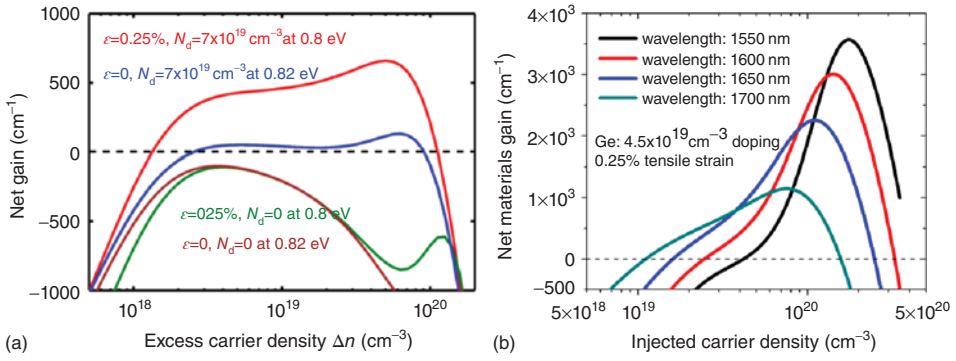

Figure 12.4 (a) Net optical gain versus injected carrier density for unstrained and tensile-strained Ge with and without n-type doping from theoretical modeling. While unstrained intrinsic Ge cannot achieve net gain, band-engineering by tensile strain and n-type can overcome this issue and achieve a large gain of 500 cm^{-1}. The FCA calculation was based on Eq. (12.6a) without taking into account BGN. © 2010 IEEE. Reprinted, with permission, from [26]. (b) Refined modeling of net gain versus injection level for 0.25% tensile-strained Ge with $n = 4.5 \times 10^{19}$ cm^{-3} at $\lambda = 1700$, 1650, 1600, and 1550 nm [39]. The model considers BGN and uses FEA from first principle model instead of Drude model. The FHA is still based on Eq. (12.6a). A broad gain spectrum from 1700 to 1550 nm is predicted for an injection level of greater than 5×10^{19} cm^{-3}. © 2013 IEEE. Reprinted, with permission, from [39].

[37] and taking into account BGN. The FHA is still modeled using the expressions in Eq. (12.6a). Net gain at 1700 nm can be achieved at an injection level of $\Delta n = 1.0 \times 10^{19}$ cm^{-3}. At higher injection levels, the net gain can be extended to shorter wavelengths. For example, at $\Delta n = 5.0 \times 10^{19}$ cm^{-3} net optical gain can be achieved in a broad wavelength range of 1550–1700 nm, and the net gain at 1650 nm can exceed 1000 cm^{-1}. Such a broad gain spectrum is suitable for on-chip wavelength division multiplexing (WDM) applications. At exceedingly high injection levels the optical gain from the direct gap transition eventually gives its way to FCA. Therefore, we can see a range of injection levels for net gain at a given wavelength.

Optical gain from Ge with >0.3% tensile strain has also been theoretically studied in recent years. Chang *et al.* [48] modeled optical gain from 0.51% tensile-strained n-type Ge QWs pseudomorphically grown on SiGeSn buffer layers with an n-type doping of 2×19^{19} cm^{-3}. They concluded that a large optical gain of ~7500 cm^{-1} can be obtained at $\lambda = 1550$ nm for transverse magnetic (TM) modes at an injected surface carrier density of 10^{13} cm^{-2}. The threshold is comparable to III–V QW lasers. El Kurdi *et al.* [32] performed an elaborate 30 band k·p modeling on highly tensile-strained Ge with in-plane tensile strain greater than 1.9%. The net gain can reach 3000 cm^{-1} at $\lambda = 3060$ nm with 3% tensile strain at an injected carrier density of $\Delta n = 1 \times 10^{18}$ cm^{-3}, exceeding the gain coefficient of GaAs at the same injection level. All these theoretical studies indicate that band-engineered Ge is a promising candidate for monolithic lasers on Si.

12.2.6
Cocktail Band-Engineering Approach Involving Sn Alloying

In addition to tensile strain and n-type doping, alloying with Sn has been developed as another approach to convert Ge into a direct band gap semiconductor in recent years [9, 49, 50]. The diamond cubic phase of Sn is known as α-Sn, and it has a negative direct band gap of −0.41 eV because the s-like Γ_7^- conduction band edge is 0.41 eV lower than the p-like Γ_8^+ valence band edge. On the other hand, the indirect gap at L valley in α-Sn is ∼0.1 eV [9, 49]. Therefore, with the increase of Sn composition the energy of the direct Γ valley decreases faster than the indirect L valleys, leading to indirect-to-direct gap transition. Based on photoreflectance and ellipsometry measurements of GeSn alloy thin films deposited on Si by chemical vapor deposition (CVD), it has been suggested that the Sn composition needed for indirect-to-direct gap transition should not exceed 11 at% for relaxed GeSn [49]. The corresponding direct band gap is ∼0.5 eV at indirect-to-direct gap transition. PL results from GeSn samples deposited on GaAs/InGaAs substrates by MBE have suggested that this transition occurs at ∼7 at% Sn for relaxed GeSn [51]. Overall, we can state that 8 – 10 at% Sn alloying is needed to convert GeSn into a direct gap semiconductor. While the equilibrium solubility of Sn in bulk Ge is only 1 at%, CVD [49], MBE [51, 52], and direct crystallization of amorphous GeSn (a-GeSn) thin films [53] all have achieved substitutional Sn compositions of ∼9 – 10 at%.

It is noteworthy that each of the three band-engineering methods mentioned above, that is, tensile strain, n-type doping, and Sn alloying, has its limitations when used alone. For the tensile strain engineering, it is very difficult to experimentally achieve 2% biaxial tensile strain or 4.6% uniaxial tensile strain that is required to transform Ge completely into a direct gap material. For n-type doping, achieving an active dopant concentration greater than 5×10^{19} cm^{-3} turns out to be challenging due to the out-diffusion of the dopants upon epitaxial growth and drive-in diffusion. For Sn alloying, achieving device-quality GeSn with >10 at% Sn concentration remains an unresolved problem.

Therefore, the most promising strategy is to find a sweet spot that incorporates intermediate levels of tensile strain, Sn alloying, and/or n-type doping, instead of stretching the fabrication capabilities for one of the methods. As an example, Figure 12.5a maps the energy difference between the indirect and direct gaps ($E_g^{\mathrm{L}} - E_g^{\Gamma}$) as a function of tensile strain and Sn composition [54]. When this number becomes positive, the material becomes a direct gap semiconductor. In this calculation, the band gaps of relaxed $\mathrm{Ge}_{1-x}\mathrm{Sn}_x$ are expressed as:

$$E_g^i(x) = (1-x)E_g^i(\mathrm{Ge}) + xE_g^i(\alpha\ \mathrm{Sn}) - b_i x(1-x); \quad i = L, \Gamma \tag{12.8}$$

where $E_g^{\Gamma}(\mathrm{Ge}) = 0.80\,\mathrm{eV}$, $E_g^{\mathrm{L}}(\mathrm{Ge}) = 0.664\,\mathrm{eV}$, $E_g^{\Gamma}(\alpha\,\mathrm{Sn}) = -0.41\,\mathrm{eV}$, and $E_g^{\mathrm{L}}(\alpha\ Sn) = 0.10$ eV. We use the bowing parameter $b_{\Gamma} = 2.0\,\mathrm{eV}$ for the direct gap [49, 51], and the upper limit of $b_{\mathrm{L}} = 1.23$ eV [49] for the indirect gap as a conservative estimate

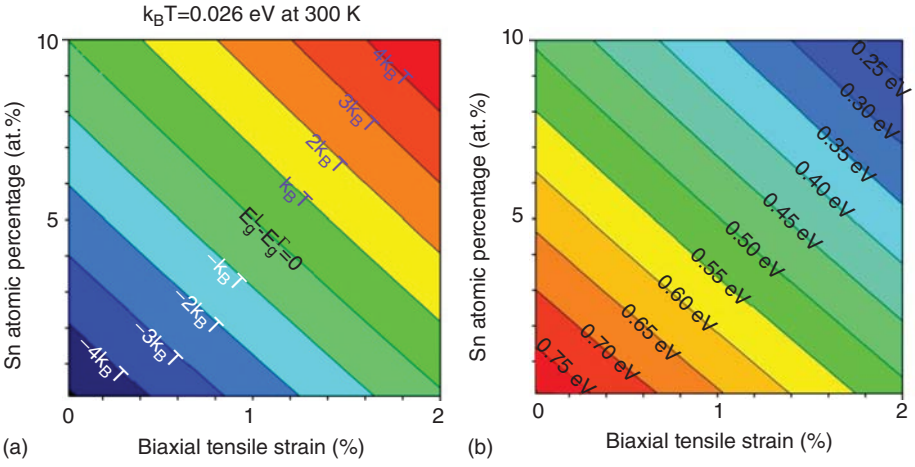

Figure 12.5 (a) Energy difference between the indirect and direct gap, $(E_g^{\mathrm{L}} - E_g^{\Gamma})$, as a function of biaxial tensile strain and Sn atomic percentage. (b) Direct band gap E_g^{Γ} as a function of biaxial tensile strain and Sn atomic concentration. Reprinted from [54] with permission under MDPI's Creative Commons Attribution License.

of the indirect-to-direct gap transition. From Eq. (12.8), the contribution of Sn alloying to the reduction in $(E_g^{\mathrm{L}} - E_g^{\Gamma})$ is

$$\Delta_{\mathrm{Sn}}(E_g^{\mathrm{L}} - E_g^{\Gamma}) = x(1.42 - 0.77x) \ \ (\mathrm{eV}) \tag{12.9}$$

We then approximate the deformation potentials of $Ge_{1-x}Sn_x$ ($x \leq 0.1$) using the corresponding parameters of pure Ge to account for the strain effect [29, 30]. The reduction in $(E_g^{\mathrm{L}} - E_g^{\Gamma})$ contributed by biaxial tensile strain, ε, is given by:

$$\Delta_{\mathrm{strain}}(E_g^{\mathrm{L}} - E_g^{\Gamma}) = 6.7\varepsilon \ \ (\mathrm{eV}) \tag{12.10}$$

As shown in Figure 12.5a,b, a small tensile strain of 0.3% and 8.6 at% Sn alloying can transform Ge into a direct gap semiconductor ($E_g^{\mathrm{L}} - E_g^{\Gamma} = 0$) with a band gap of ~0.5 eV. This calculated result is in very good agreement with Li *et al.*'s [53] recent experimental data on a 0.3% tensile-strained $Ge_{0.913}Sn_{0.087}$ sample. Further considering the thermal excitation energy at 300 K, the material can already be regarded as a direct gap when $E_g^{\Gamma} - E_g^{\mathrm{L}} \sim k_{\mathrm{B}}T = 0.026$ eV. For 0.3% tensile strain, this can be achieved at 7 at% Sn alloying. If the tensile strain can be moderately engineered to 0.6%, only 5 at% Sn alloying is needed to achieve the indirect-to-direct gap transition effectively. As will be shown in the next section, both can be readily implemented using existing strain and Sn alloying technologies. Even for $E_g^{\Gamma} - E_g^{\mathrm{L}} = 2k_{\mathrm{B}}T = 0.052$ eV, the n-type doping required to compensate for the energy difference between the direct and indirect gap is significantly reduced to $\sim 2 \times 10^{19}$ cm^{-3}, compared to 7.6×10^{19} cm^{-3} originally proposed by Liu *et al.* [15]. The lower n-type doping not only helps to reduce the detrimental Auger recombination, but also simplifies the materials growth

process. In addition, as will be shown in Section 12.3, such a pseudo-direct gap configuration can increase the emission efficiency at high temperature and high injection levels due to enhanced L-to-Γ valley excitation or scattering [44, 46, 56–58]. Thus, one can also optimize the relative positions of L versus Γ valley for high power on-chip laser sources, where high injection current and high thermal stability up to 80 °C are required. The small band gap of tensile-strained GeSn shown near the top right corner of Figure 12.5b also indicates that it has significant potential applications in Si-based mid infrared integrated photonics.

12.2.7
Toward High Performance Ge QW Structures

In addition to directly engineering the Ge material itself, we proposed that the band structure of Ge could also be engineered toward the direct gap semiconductor by carefully designing the QW device structures [39]. QWs are commonly applied in LDs to reduce the threshold current density and increase quantum efficiencies. Theoretical investigations on direct gap Si/Ge superlattices and QWs have started since the 1980s [59] and have continued through recent years [60, 61]. However, there has been no experimental demonstration of direct gap SiGe QW structures so far. A couple of challenges have to be addressed. Firstly, in SiGe/Ge QWs the quantum confinement actually increases the energy difference between the direct and indirect gaps due to the much smaller effective mass and much deeper well seen by Γ electrons, as shown in Figure 12.6a. Secondly, the epitaxial growth of Ge on SiGe typically results in compressive strain in Ge due to the lattice mismatch, which also increases the energy difference between Γ and L valleys.

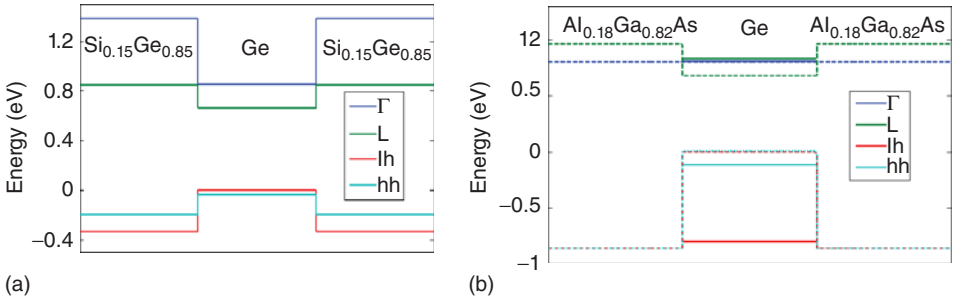

Figure 12.6 (a) $Ge_{0.85}Si_{0.15}$/Ge/$Ge_{0.85}Si_{0.15}$ QW band structure assuming 0.25% tensile strain in an 11.8 nm thick Ge QW. (b) Band structures of an AlGaAs/Ge/AlGaAs QW for separate electron confinement in L and Γ valleys assuming no strain (due to nearly perfect lattice matching). The thickness of Ge is 3.3 nm. For different valleys, dashed lines show the band edges and solid lines show the first energy level in the wells. Barrier material is chosen so that there is little quantum confinement in Γ valley but significant confinement in L valley. © 2013 IEEE. Reprinted, with permission, from [39].

In order to improve the Ge QW structures, Cai *et al.* proposed a "separate electron barrier" approach [39], where the barrier material provides strong confinement in the L valleys, but weak confinement in the Γ valley. This idea can be implemented by carefully choosing the barrier material that provides a large band-offset in L valleys while small offset in Γ valley with Ge (Figure 12.6b). Such band alignment can make Ge "direct band gap" by raising the L valleys above the Γ valley due to the stronger quantum confinement of electrons in the L valleys. As an example, the band diagram of an AlGaAs/Ge/AlGaAs QW structure is shown in Figure 12.4b, where the Ge QW is converted into a direct gap semiconductor due to the stronger quantum confinement of electrons in the indirect L valleys provided by the AlGaAs barriers. One could also tweak the design to engineer the L valley slightly below the Γ valley for high lasing performance at elevated temperatures, as mentioned earlier. There are several advantages of this approach: (i) The AlGaAs barrier layer is not an active material but just a barrier layer electrode, so it can be deposited at low temperatures to avoid diffusion of III and V elements and achieve CMOS compatibility. (ii) Off-cut wafers may not be needed either, because antiphase boundaries will not significantly affect the performance in this case. (iii) Pseudo-direct gap Ge lasers offer much better thermal stability, and in this case one can engineer the relative positions of L and Γ valleys by QW design for optimal performance. In III–V lasers, quantum dot (QD) lasers also show good thermal stability, but the wavelength of these QDs is far from 1550 nm and they have not been integrated on Si so far. Therefore, this new Ge QW design could offer a simple solution to high-performance monolithic lasers on Si at 1500–1700 nm.

In the case of tensile-strained Ge or GeSn active gain media, the energy gap reduction due to tensile strain and/or Sn alloying can also be partially compensated by the quantum confinement effect. This compensation helps to avoid potential issues related to the dark current in small band gap semiconductors.

12.3 Fabrication of Band-Engineered Ge-on-Si

Now that theoretical analyses and modeling demonstrate the feasibility of optical gain and lasing from band-engineered Ge-on-Si, high quality material growth is the first critical step to implement the device experimentally. The greatest challenge for high- quality Ge epitaxy on Si is the 4.2% lattice mismatch between these two materials.

To achieve device quality epitaxial Ge on Si without using very thick SiGe buffer layers, a two-step direct Ge growth technique is applied to prevent Stranski–Krastanov growth [62, 63], and subsequent annealing was developed to decrease the threading dislocation density below 10^7 cm^{-2} [64]. In the initial growth step, a thin epitaxial Ge buffer layer of 30–60 nm is directly grown on Si at 320–360 °C. At such a low growth temperature islanding of Ge associated with Stranski–Krastanov growth is kinetically suppressed due to the low surface diffusivity of Ge. In the main growth step, the growth temperature is increased

to >600 °C for higher growth rates and better crystal quality. A post-growth annealing at >750 °C can reduce the threading dislocation density from 10^9 to 10^7 cm^{-2}. In selectively grown Ge mesas with lateral dimensions ~10 μm, the threading dislocation density can be further reduced to 10^6 cm^{-2} because these dislocations can glide to the edge of the mesas and annihilate [64]. This method is by far the most popular approach for epitaxial Ge-on-Si growth.

More recently, the rapid melting growth (RMG) or liquid phase epitaxy (LPE) of Ge has been developed as an alternative to MBE and CVD epitaxy [55, 65, 66]. In this case an amorphous Ge (a-Ge) thin film is deposited on a dielectric layer with a small window in contact directly with the single crystalline Si substrate to serve as the seedling region for the single crystal Ge growth upon melting and recrystallization. The a-Ge deposition does not require MBE or CVD epitaxy tools, so it can be implemented by less costly, higher throughput methods such as plasma enhanced chemical vapor deposition (PECVD).

In the following text we will focus on three critical aspects related to band-engineered Ge-on-Si lasers: (i) introduction and enhancement of tensile strain, (ii) n-type doping, and (iii) Sn alloying. The readers are also referred to Chapters 3 and 4 of this book for more details on heavy doping and growth of tensile-strained Ge.

12.3.1
Tensile Strained Ge-on-Si

When we consider Ge epitaxy on Si, a common impression is that *compressive* strain would be introduced to Ge during pseudomorphic growth because the lattice constant of Ge is larger than that of Si. However, this is not the case for relatively thick epitaxial Ge layers on Si for photonic devices. The thickness required in optical devices is on the order of λ/n_r, where λ is the wavelength and n_r is the real part of the refractive index. For Ge photonic devices operating at $\lambda = 1550$ nm the thickness is thus in the order of several hundred nanometers. This thickness far exceeds the critical thickness for pseudomorphic growth of Ge on Si, so the Ge film is relaxed at growth temperatures >600 °C. Upon cooling to room temperature, *tensile strain,* instead of compressive strain, can be accumulated in the Ge layers due to the larger thermal expansion coefficient of Ge compared to Si [67–69]. Typically 0.2–0.3% tensile strain can be achieved using this process, which reduces the difference between the direct and indirect band gaps of Ge from 136 to ~100 meV and red-shifts direct band gap from 0.8 to 0.76 eV [30, 44, 56, 70]. Recently, a thermally induced tensile strain of 0.4% has been reported from GeOI grown by RMG/LPE [71] due to the high growth temperature and reduced stress relaxation upon fast cooling after rapid thermal annealing (RTA). One of the challenges for Ge laser applications, though, is that the Ge region almost inevitably incorporates a small amount of Si due to Ge–Si inter-diffusion upon melting. Incorporation of Si increases the energy difference between the direct and indirect band gaps. More details about tensile strained Ge growth can be found in Chapter 10.

To further enhance the tensile strain in epitaxial Ge, in recent years relaxed GeSn buffer layers on Si have been developed as a lattice template for tensile-strained Ge [72, 73]. This approach has achieved up to 0.68% tensile strain [74]. Stressor layers such as silicides [55, 75] or silicon nitride [76, 77] have also been proved effective in enhancing the tensile strain in Ge.

An alternative approach to tensile-strained Ge is directly applying external mechanical stress. Lim *et al.* [78] proposed a micromechanical structure for introducing tensile stress to Ge light emitters. El Kurdi *et al.* applied external stress to bulk Ge wafer and demonstrated 0.6% tensile strain, leading to a red-shift of the direct gap emission peak from 1535 to 1660 nm [79]. Cheng *et al.* reported a 1.8× enhancement of direct gap PL for 0.37% tensile strain mechanically applied on bulk Ge [80]. For device applications, micro-electromechanical systems (MEMS) may be coupled with suspended thin Ge layers to achieve enhanced tensile strain in Ge light emitters. Recently, Jain *et al.* [81] have demonstrated a prototype MEMS device with up to 1.4% uniaxial and 1% biaxial tensile strain introduced to a suspended Ge layer by a Si_3N_4 stressor (Figure 12.7a–c). Compared to bulk Ge, the PL peak red-shifts to $\lambda = 1860$ nm ($h\nu = 0.64$ eV) and the integrated intensity increased by 260 times. Süess *et al.* [82] achieved 3.1% uniaxial tensile strain in a suspended Ge beam by patterning and under-etching 0.15% tensile-strained Ge thin films grown on Si and silicon-on-insulator (SOI) substrates (Figure 12.7d–f). This approach utilizes the fact that, at a constant force in the plane of the Ge films, the stress is inversely proportional to the cross-sectional area of the suspended structures. Because the suspended beam can be patterned into a very small cross-section, the stress in this region is greatly enhanced compared to the blanket film regime. The direct band gap shrinks by 0.21 eV to $h\nu = 0.59$ eV ($\lambda = 2100$ nm) in this case, and the PL intensity increases by 25 times. Further increase in tensile strain is only limited by the mechanical strength of Ge itself. Indeed, very lately the same group has further achieved 4% uniaxial strain [83], while Sukhdeo *et al.* [84] have reported 5.7% tensile strain along <100> direction. In addition, Capellini *et al.* [85] have reported up to ~0.9% equivalent biaxial tensile strain in a SiN(stressor)/Ge/SOI(001) stack using 130 nm bipolar-CMOS (Bi-CMOS) processing.

12.3.2 N-Type Doping

As shown earlier, n-type doping is another critical factor to achieve efficient light emission from the direct gap transition of Ge. Table 12.1 summarizes the solubility of n-type dopants in Ge [16]. According to these data, phosphorous is the best n-type dopant for Ge due to the largest solubility in the widest temperature range. One should note, however, that non-equilibrium growth methods such as delta doping and MBE could achieve doping levels exceeding the solubility limit. A particular challenge, though, is that n^+ doping has to be implemented without introducing non-radiative recombination centers. Although ion implantation is widely applied for doping processes in CMOS circuits, the defects induced by

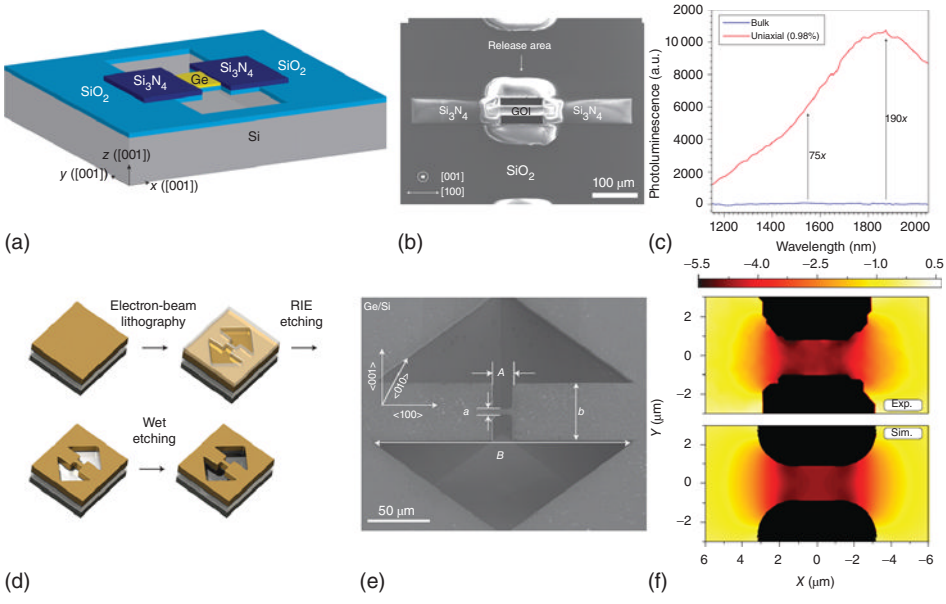

Figure 12.7 Upper part: a micromachining-based suspension platform for highly tensile-strained Ge reported by Jain *et al.* [81]: (a) schematics of the device structure using Si_3N_4 stressors on suspended Ge, (b) Scanning electron microscopy (SEM) image of the device, (c) micro PL spectrum of 0.98% uniaxially strained Ge shows a significant red-shift of peak position and increase in peak intensity. Lower part: highly tensile-strained Ge microbeams reported by Süess *et al.* [82], (d) Schematics of the suspended Ge microbeam fabrication process, (e) SEM photo of the Ge microbeam structure. The microbeam has a length of A and a width of *a*, and (f) Micro-Raman mapping of the suspended Ge microbeam (upper panel) and its comparison with theoretical modeling (lower panel). The maximum Raman shift of $-4.8\,cm^{-1}$ corresponds to a uniaxial tensile strain of 3.1%. Reprinted with permission from Macmillan Publishers Ltd: NATURE PHOTONICS [81, 82], © 2012–2013.

Table 12.1 Solubility of different n-type dopants in Ge [16].

Dopant	Maximum solubility	Temperature dependence
P	$2\times10^{20}\,cm^{-3}$ @580 °C	$>1\times10^{20}\,cm^{-3}$, 500–800 °C
As	$8.7\times10^{19}\,cm^{-3}$ @800 °C	$>8.0\times10^{19}\,cm^{-3}$, 750–880 °C
Sb	$1.1\times10^{19}\,cm^{-3}$@800 °C	$>1.0\times10^{19}\,cm^{-3}$, 750–870 °C

high-energy ion bombardment is not suitable for light-emitting devices [86]. To minimize defect formation, three approaches have been developed for heavy n-type doping in Ge: (i) regular *insitu* doping [44, 47, 58, 86, 87], (ii) delta doping followed by thermally activated drive-in diffusion [88–91], and (iii) diffusion doping from spin-on dopant (SOD) sources [92].

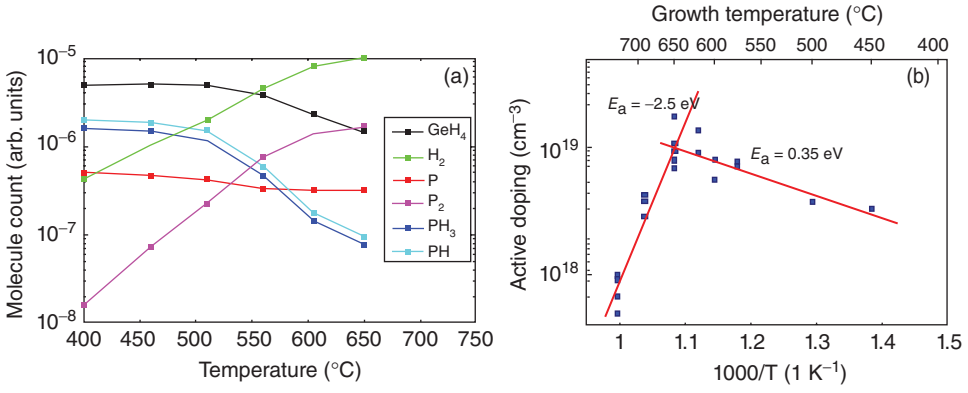

Figure 12.8 (a) Relative counts of different gas species during the epitaxial growth of *in situ* doped n-type Ge. (b) Arrhenius plot of active n-type dopant concentration versus growth temperature. Reprinted from [92], with permissions from Elsevier © 2012.

12.3.2.1 Regular *In situ* Doping

For *insitu* doping, PH_3 is used as the precursor during CVD growth [44, 57, 86, 87] while Sb has been adopted for n-type doping in MBE growths [47, 58]. In CVD the optimal growth temperature is typically 600–700 °C to achieve up to 2×10^{19} cm^{-3} *activated* P concentration without sacrificing crystal quality [27, 92]. Although higher P *atomic* concentration can be incorporated at lower growth temperatures of ~400 °C, the material quality and dopant activation are adversely affected [87] due to lack of atomic diffusion. On the other hand, if the growth temperature is above 750 °C P atoms in Ge tend to out-diffuse and evaporate into the gas phase (P_2 gas molecules) and reduce n-type doping concentration. As an example, Figure 12.8a shows the relative molecular counts of different gas species in the ultrahigh vacuum chemical vapor deposition (UHVCVD) reactor during *in situ* n-type Ge growth, as measured by a residual gas analyzer [92]. With the increase of temperature, PH_3 precursor starts to break down so the pressure of PH_3 decreases with temperature. Correspondingly, the partial pressure of P_2 gas molecules increases with temperature. Therefore, in the CVD process the incorporation of P into Ge is determined by the equilibrium between P dopants in Ge (solid phase) and P_2 gas phase. Figure 12.8b shows an Arrhenius plot of active dopant concentration versus growth temperature. The active phosphorous doping concentration was measured by the Hall effect from n^+ Ge films grown on p^- Si substrates. This method guarantees that carrier transport is dominated by the n^+ Ge layer so that carrier density and mobility are measured for the n^+ Ge film only. We found that a growth temperature of ~650 °C is optimal for the UHV-CVD n^+ Ge growth. Below this temperature, phosphorous concentration is mainly limited by PH_3 decomposition; above this temperature, phosphorous in Ge tends to out-diffuse and evaporates into the gas phase (P_2 gas molecules). An active n-type doping concentration of $\sim2\times10^{19}$ cm^{-3} has been achieved by *in situ* doping.

In MBE growths the Sb doping was performed at a low temperature of ~350 °C and a doping level up to 10^{20} cm^{-3} was demonstrated. A notable difference from

n^+ Ge grown by CVD is that the Ge film is relaxed rather than tensile-strained due to the low MBE growth temperature, that is, thermally induced tensile strain almost exactly cancels the residual compressive lattice strain in this case.

12.3.2.2 Delta Doping Followed by Thermally Activated Drive-in Diffusion

To further increase the active n-type doping level in CVD growth without deteriorating material quality, Camacho-Aguilera *et al.* [89, 90] deposited a stack of delta-doped Ge/P layers at low temperatures (400–450 °C) on top of regularly *in situ* doped Ge, and then annealed the samples to drive-in the dopants (Figure 12.9a). The stack of delta doped Ge layers consisted of alternating monolayers of P and

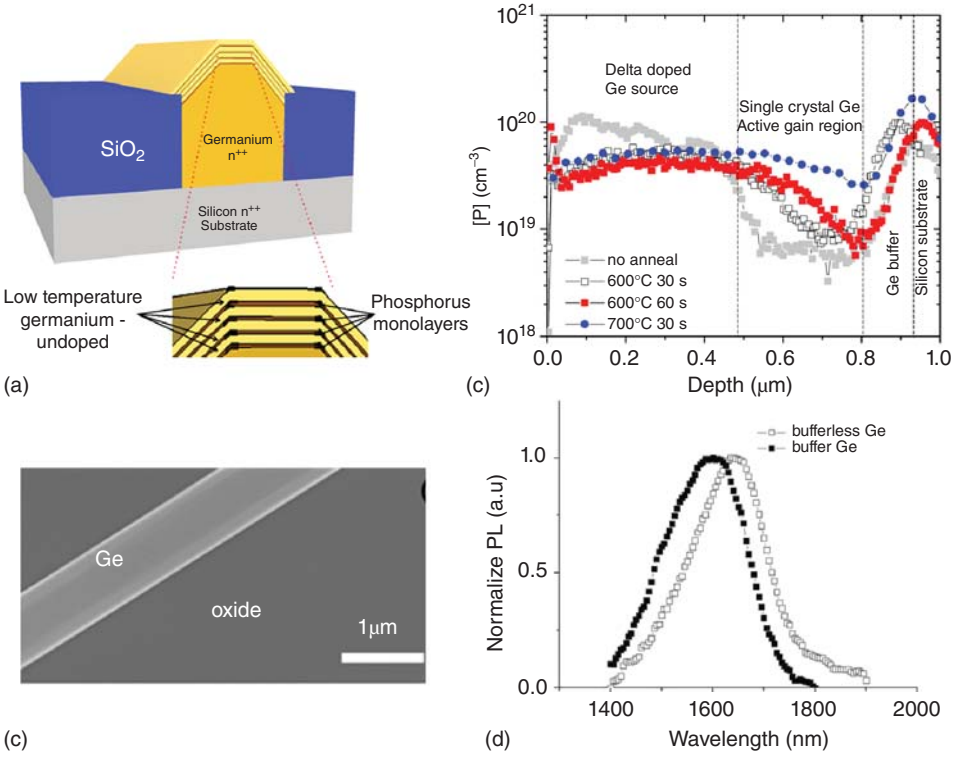

Figure 12.9 (a) Schematics of the delta-doped Ge/P stacks as a drive-in diffusion source. Courtesy of Dr Jurgen Michel, Massachusetts Institute of Technology. (b) Secondary ion mass spectroscopy (SIMS) of P distribution profiles for unannealed and annealed samples. Approximately 4×10^{19} cm^{-3} doping level can be achieved after RTA at 700 °C for 30 s. Reprinted from [90] with permission from the OSA. (c) Buffer-less Ge growth in narrow trenches, demonstrating uniform growth. The facets indicate the single crystal nature of Ge. (d) PL spectra of buffered and bufferless Ge samples with the same tensile strain. The red-shift in PL peak position of the bufferless sample indicates a higher active n-type doping resulting from BGN. This is enabled by alleviating the dopant segregation at the Ge/Si interface. Reprinted with permission from [93], © 2012, the Electrochemical Society (ECS).

undoped Ge layers. The reason not to use *in situ* doped n-type Ge layers in this stack is that the growth rate of the doped Ge is very low when deposited on the P delta layers at low temperatures. The integrated concentration of P in the delta layer stack was well above 10^{20} cm^{-3} and could therefore be used as a P source for drive-in diffusion. Owing to the high P doping level in the regularly *in situ* doped n-type Ge, dopant-enhanced diffusion leads to a diffusivity two orders higher than intrinsic Ge. This high diffusivity enables short drive-in diffusion times that can be implemented by RTA, reducing P out-diffusion at the surface [91]. As shown in Figure 12.9b, after RTA at 700 °C for 30 s an n-type doping level of $\sim 4 \times 10^{19}$ cm^{-3} can be achieved in the active Ge region. Note that the delta doped stack itself is of low crystallinity because the P monolayers disrupt the single crystal growth and poly Ge is formed. Therefore, it is used as a diffusion source only and is removed by chemical mechanical polishing (CMP) after the drive-in diffusion process [94].

An issue identified for n^+ Ge-on-Si fabrication is that the highly dislocated low-temperature Ge buffer layer becomes an undesirable sink for the dopants in n^+ Ge (Figure 12.9b) and one of the limiting factors of carrier lifetime [95]. While the buffer layer is necessary for blanket film growth, this step can actually be skipped for selective growths in narrow trenches ≤ 1 μm in width [93, 96] without affecting the growth profile or trench filling (Figure 12.9c). This is because the trench width is even smaller than the size of the Ge islands that would spontaneously form upon Stranski–Krastanov growth, providing effective stress relaxation due to the geometrical confinement. With the strain energy already reduced, it is no longer necessary to form islands along the trenches as this would increase the surface energy. This method could improve the material quality at the Ge/Si interface and enhance the carrier injection efficiency in Ge lasers. It has been demonstrated that at the same tensile strain level, the bufferless Ge grown in narrow trenches show a red-shift in the PL spectra, indicating more BGN due to a higher active dopant doping level by alleviating the dopant segregation at the Ge/Si interface (Figure 12.9d).

12.3.2.3 Diffusion Doping from SOD Sources

For process integration of photonic devices, it is desirable to locally dope designated Ge regions for light-emitting devices so that other regions can remain intrinsic for Ge photodetector and electro-absorption modulators. Based on this motivation, SODs have been developed as an alternative approach to achieve n^+ doping in Ge [92]. After coating SOD on epitaxial Ge films, the samples are baked and ashed to remove solvents and any organic components so that only P-doped SiO_2 is left on the Ge surface. A SiN layer is deposited on top to help prevent out-diffusion of phosphorous upon drive-in annealing. After RTA at greater than 700 °C, an average doping concentration up to 2×10^{19} cm^{-3} can be achieved in initially intrinsic Ge films. The trade-off in this case is drive-in diffusion into Ge versus out-diffusion of phosphorous dopants. Both *in situ* doping and diffusion doping from SOD have achieved strong room temperature PL from the direct gap transition of Ge, which is ~10 times higher than implanted samples with the same phosphorus doping concentration.

12.3.3 Sn Alloying

Epitaxy of GeSn has been implemented by both MBE and CVD. The development of SnD_4 precursor was the key factor that enabled Sn alloying in CVD growth [97]. The deposition temperature is typically between 200 and 350 °C, and higher Sn content typically requires lower growth temperature to prevent Sn segregation. Compared to Ge, GeSn tends to relax more easily on Si substrate due to an even larger lattice mismatch. Similar to epitaxial Ge, annealing has been shown to improve the optoelectronic properties of GeSn [51, 98] by reducing the defect density. RTA is preferred in this case to remove the defects without causing Sn segregation. Because room-temperature light emission has been demonstrated from both MBE and CVD growth samples, there does not seem to be a significant difference in material quality between these two epitaxial growth methods. It is also noteworthy that up to 25 at% Sn alloying has been demonstrated recently using MBE at a very low growth temperature of 120 °C [99]. The thickness of the $Ge_{0.75}Sn_{0.25}$ thin film is limited to 50 nm before the epitaxy breaks down.

Another approach to alloy Sn with Ge is to crystallize a-GeSn thin film materials. This method is based on the consideration that Sn and Ge form a eutectic system with a low eutectic temperature of 231 °C, which facilitates low-temperature crystallization upon annealing because the Sn-rich liquid phase enhances atomic transport. A significant benefit is that the GeSn growth does not require single crystal Si substrate to provide a template, and it can be implemented on any dielectric layers to achieve 3D photonic integration. Moreover, without lattice mismatch with Si, the GeSn grown on dielectric layers could be free of dislocation defects. The a-GeSn thin films can be deposited on dielectric layers by co-evaporation. High crystallinity blanket GeSn thin films on SiO_2 with up to 8.7 at% Sn and 0.3% tensile strain has then been achieved by crystallization annealing at ∼460 °C [53]. According to Figure 12.5, this material is a direct band gap semiconductor already. The measured band gap of ∼0.5 eV from optical transmittance spectroscopy (Figure 12.10a) is in good agreement with the theoretical calculation in Figure 12.5. Remarkably, Figure 12.10b,c clearly identified nucleation centers that are as far as ∼0.1 – 1 mm away from one another, from which the grains grow radially. This striking observation is highly unusual in the crystallization of amorphous semiconductor thin films, and it suggests an extraordinarily fast lateral grain growth rate versus a slow nucleation rate during the eutectically enhanced crystallization process of GeSn. Electron backscatter diffraction (EBSD) analysis shows that the average grain size is as large as ∼10 μm, and the majority of grain boundaries are relatively benign twin boundaries (Figure 12.10d,e). For an initial Sn composition of 9 – 13 at% in the as-deposited films, the crystallized GeSn film exhibits a strong (111) texture, as shown by the inverse pole figure in the inset of Figure 12.10e. The excess Sn from the solidification of the Sn-rich liquid phase segregates on the surface of the GeSn thin films along the small angle grain boundaries, and it can be selectively removed by a 37% HCl:H_2O solution with a high Sn-to-GeSn (Ge-rich) etching selectivity >4800 : 1. Further employing

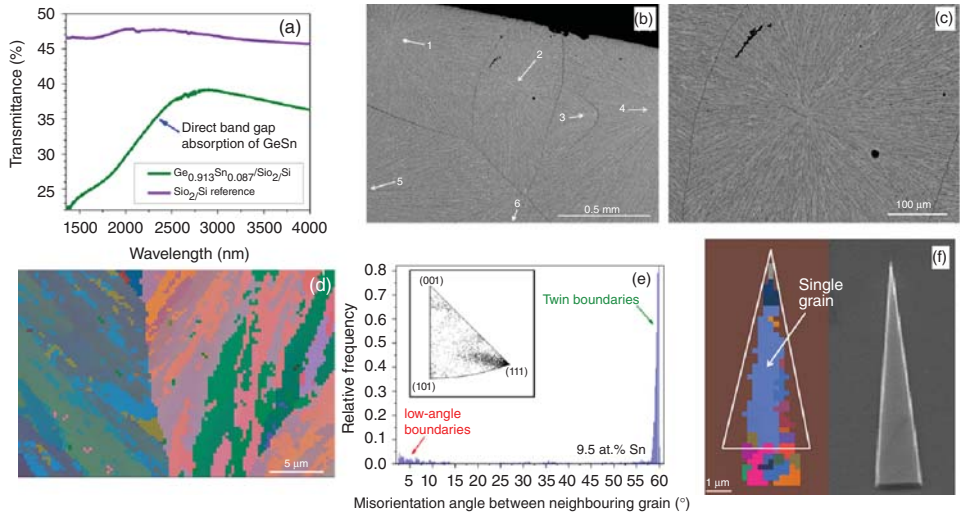

Figure 12.10 (a) Transmittance spectrum of a high crystallinity 0.3% tensile-strained $Ge_{0.913}Sn_{0.087}$ thin film sample crystallized from a-GeSn with 9.5 at% Sn on SiO_2. The data of a reference sample without the GeSn thin film is also shown for comparison. The onset of strong absorption at $\lambda = 2500$ nm is consistent with the calculated direct band gap of ~0.5 eV in Figure 12.5. (b) Large-area SEM image of the crystallized $Ge_{0.913}Sn_{0.087}$ thin film. The arrows point to six nucleation centers in a total area of ~1.6 mm^2, from which GeSn grains grow radially. The scale bar is 0.5 mm. (c) A zoomed-in image of domain 2 in (b). The scale bar is 100 μm. (d) EBSD mapping of the crystallized GeSn thin film, where different colors indicate different in-plane crystallographic orientations. The scale bar is 5 μm. (e) Distribution of misorientation angles between neighboring grains derived from the EBSD data. The inset shows an inverse pole figure obtained over a 0.2 mm × 0.2 mm area, indicating a strong (111) texture. (f) A crystallized patterned $Ge_{0.913}Sn_{0.087}$ taper structure on SiO_2 (right) and its EBSD mapping (left). The taper structure is dominated by a single grain, with the rest of the grains forming twin boundaries with it. Reprinted form [53] under the Author's Copyright Transfer Agreement with the OSA.

geometrically confined growth in patterned structures, pseudo single crystalline GeSn is achieved on SiO_2 layers, as shown in Figure 12.10f [100, 101]. Here, a large grain dominates the structure, and all the boundaries are identified to be twin boundaries. The GeSn films can also be crystallized on glass or polyimide substrates in a similar fashion. These results show that it is promising to achieve direct gap GeSn patterns for active photonic device integration on *any* dielectric layers.

12.4 Band-Engineered Ge-on-Si Light Emitters

With high-quality band-engineered Ge-on-Si materials, light emission properties of Ge are expected to improve significantly. In this section we will present

spontaneous emission, optical gain, and lasing from these materials, and discuss the on-going work on electrically pumped Ge-on-Si lasers.

12.4.1 Spontaneous Emission

12.4.1.1 Features of Direct Gap Emission from Ge

Although direct gap PL of intrinsic and heavily doped bulk Ge has been studied in several papers between the 1960s and 1980s [19–24], a systematic approach on the direct radiative transition of epitaxial Ge-on-Si band-engineered by tensile strain and/or n-type doping did not start until recent years. Direct gap spontaneous emission in Ge, regardless of PL or electroluminescence (EL), exhibits three distinct features that are exactly *opposite* to the behavior of conventional direct gap III–V semiconductors:

1) The integrated emission intensity *increases* with *n-type doping level* [44, 46, 57, 86], as shown in Figure 12.3a. The integrated PL intensity at room temperature increases by more than 100 times with 3×10^{19} cm^{-3} active n-type doping compared to intrinsic Ge-on-Si, consistent with our theoretical model on enhanced direct gap emission by filling L valleys with extrinsic electrons from n-type doping [44, 46].
2) At high injection levels the spontaneous emission intensity increases *superlinearly* with injection current [47, 56–58] or optical pumping power [21, 81], as shown in Figure 12.11.
3) The emission intensity *increases* with *temperature* [44, 57], as shown in Figure 12.12. The PL intensity keeps increasing up to ~100 °C (373 K) [46].

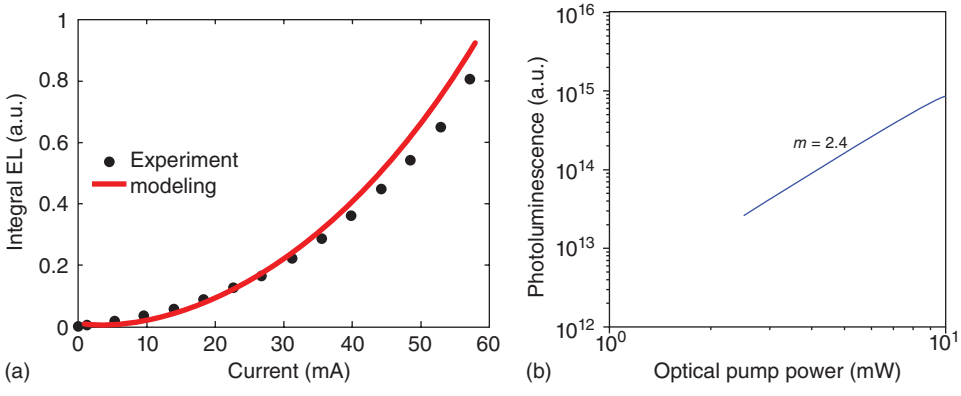

Figure 12.11 (a) Integrated EL intensity versus injection current of a 0.2% tensile strain Ge-on-Si LED [56]. The EL intensity increases superlinearly with injection current. Reprinted from [56] under the Author's Copyright Transfer Agreement with the OSA. (b) Log-log plot of PL intensity versus optical pump power. The exponent of $m = 2.4$ indicates superlinear increase of PL intensity with pump power. Reprinted with permission from Macmillan Publishers Ltd: NATURE PHOTONICS [81], © 2012.

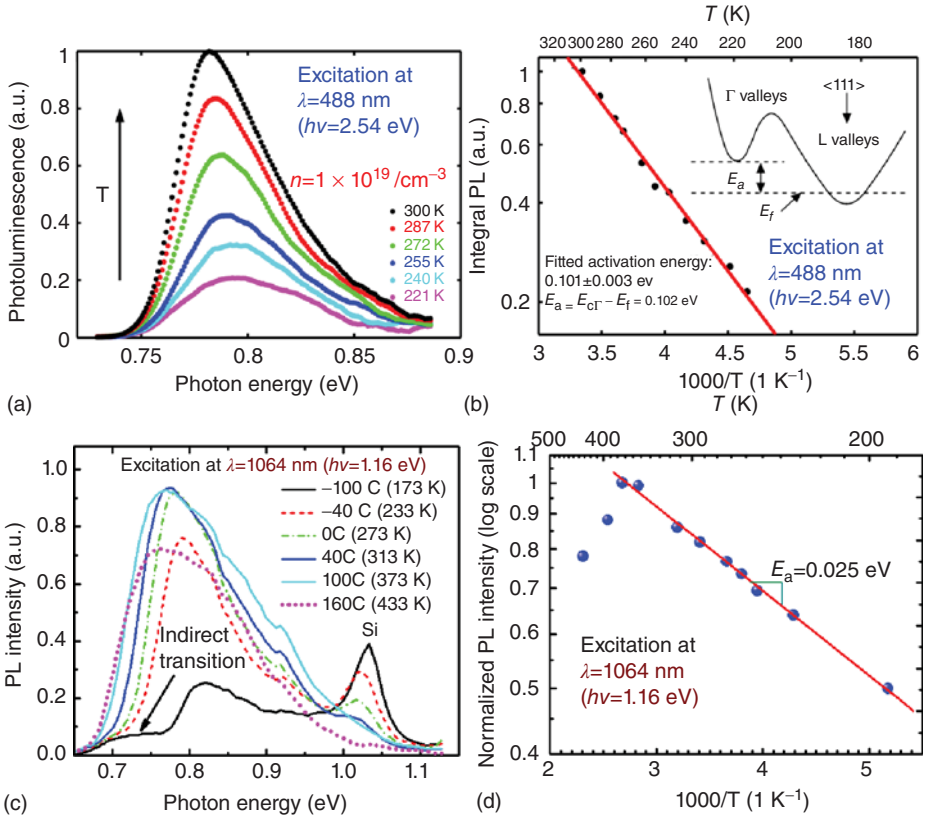

Figure 12.12 PL spectra (a,c) and integrated PL intensity versus temperature (b,d) for 0.25% tensile-strained Ge on Si with $n = 1 \times 10^{19}$ cm^{-3}. (a) and (b) are excited at $\lambda = 488$ nm ($hv = 2.54$ eV), while (c) and (d) are excited at $\lambda = 1064$ nm ($hv = 1.16$ eV). Both cases show an increase of PL intensity with temperature, yet at 488 nm excitation the activation energy is much higher than that at 1064 nm. This is because 488 nm light preferably pump electrons to the indirect L valleys so that electronic occupation of direct Γ valley requires thermal excitation. As a result, the activation energy is equal to the difference between the Γ valley and the Fermi level. On the other hand, 1064 nm light preferably pump electrons directly into the Γ valley, so the direct gap PL intensity depends much less on thermal excitation from the L valleys. Panels (a) and (b) are reprinted from [44] with permissions from AIP Publishing, LLC.

These unusual phenomena are because the energy states in direct Γ valley are higher than those in indirect L valleys. The direct gap luminescence intensity is proportional to the number of injected electrons in the Γ valley, $\Delta n_e(\Gamma)$, which is the product of the total injected electron concentration, $\Delta n_e(\text{total})$, and the faction of the electrons in the Γ valley, $f(\Gamma)$:

$$\text{Emission}_{\text{dir}} \propto \Delta n_e(\Gamma) = \Delta n_e(\text{total}) f(\Gamma) \tag{12.11}$$

At a constant injection level, that is, constant Δn_e(total), increasing n-type doping concentration raises the Fermi level so that the fraction of electrons occupying the higher energy Γ valley, $f(\Gamma)$, will increase, leading to enhanced direct gap emission. Similarly, thermal excitation promotes electrons from L valleys to higher energy states in the Γ valley. As a result, the increase in temperature also enhances light emission via direct transition. The PL intensity decrease at >393 K (120 °C) is likely due to thermally activated non-radiative recombination centers and/or further excitation of electrons from Γ into the higher energy indirect Δ valleys. When the excitation intensity increases, Δn_e(total) scales linearly with the injection level, while $f(\Gamma)$ also increases with the injection level owing to the increase of the quasi-Fermi level. The multiplication of these two terms in Eq. (12.11) results in a superlinear increase of direct gap emission with excitation level (Figure 12.11). The increase in emission efficiency with injection level and temperature are especially attractive for high power on-chip laser sources where high injection current and high thermal stability up to 80 °C are required in electronic–photonic integrated circuits.

Another notable feature of the spontaneous emission from Ge is that the PL spectra and their temperature-dependent intensity can be drastically influenced by the excitation photon energy. Wagner and Viña [24] showed that the PL intensity ratio of the direct-to-indirect gap transitions at 5 K from unstrained p^+ Ge is highly dependent on the excitation photon energy. As the excitation photon energy decreases from 2.4 to 0.9 eV, the intensity ratio of direct to indirect PL drastically increases by three orders of magnitude from ~0.01 to ~10 (Figure 12.13a). This is because high- energy photons >2 eV can directly excite electrons from deep

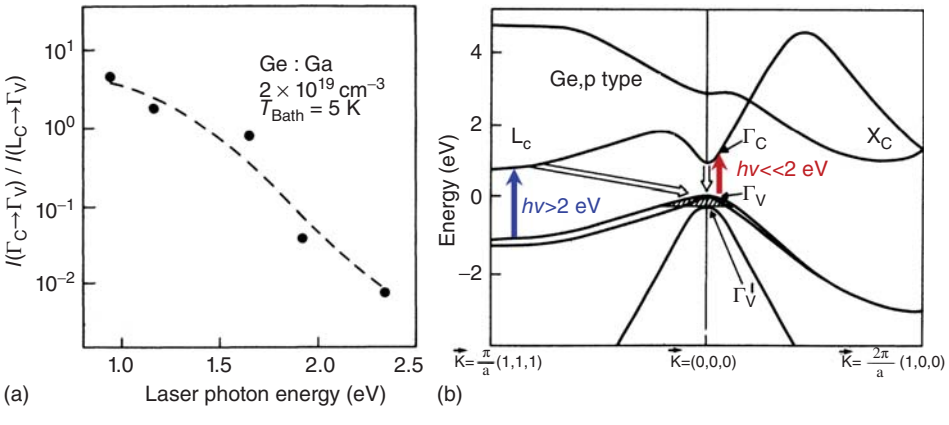

Figure 12.13 (a) The ratio of direct gap to indirect gap PL intensity as a function of pump laser photon energy at $T = 5$ K for p^+ Ge with $p = 2 \times 10^{19}$ cm^{-3}. Clearly, lower pumping photon energy favors direct gap PL. (b) Schematic band diagram of Ge explaining the observation in (a). High energy photons can directly pump electrons from deep inside the valence band into the L valley, which favors indirect gap transition. Lower energy photons are more likely absorbed by the direct gap transition and pump electrons into the Γ valley. Figures reprinted from [24] with the copyright permission from the APS.

inside the valence band into the L valley (Figure 12.13b), while lower energy photons are much more likely to be absorbed by direct gap transition and populate the Γ valley as long as their energy is greater than the direct band gap. Therefore, pumping photon energy close to the direct gap is preferred for investigating the direct gap light emission and optical gain. This mechanism also leads to the drastically different activation energies in the Arrhenius plots of PL versus temperature for 0.25% tensile-strained n^+ Ge-on-Si shown in Figure 12.12b,d. Under 488 nm laser excitation, electrons are preferably pumped into the indirect L valleys. Some carriers can be thermally excited from the L valleys to the direct Γ valley. Therefore, the measured activation energy in Figure 12.12b is equal to the energy difference between the Γ valley and the Fermi level. On the other hand, the 1064 nm excitation laser preferably pumps electrons directly into the Γ valley, leading to less dependence on the thermal excitation from L valleys and a much lower activation energy. Further investigations on the dependence of PL on the

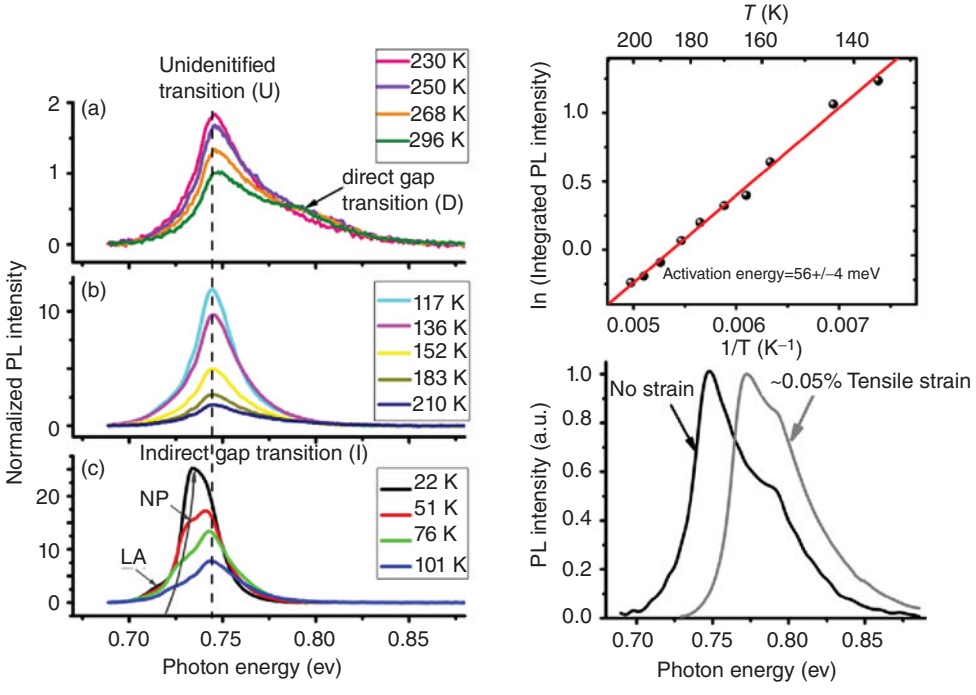

Figure 12.14 PL spectra of a 10^{16} cm^{-3} arsenic doped single crystal Ge sample in the temperature ranges of (a) 230–296 K, (b) 117–210 K, and (c) 22–101 K. The peak at 0.74 eV is neither from the indirect nor direct gap transition. This unidentified peak is labeled as "U" in the figure. (d) An Arrhenius plot of the integral intensity of peak U in the temperature range of 130–210 K. An activation energy of 56 ± 4 meV is obtained. (e) PL spectra of 10^{16} Ga-doped single crystal Ge under 0 and ~0.05% externally applied tensile strain. Peak U blue-shifts by ~25 meV under 0.05% tensile strain, opposite to the behavior of direct and indirect gap band-to-band transitions. Reprinted from [102] under the Author's Copyright Transfer Agreement with the OSA.

excitation photon energy may reveal more details about the carrier distribution between the direct and indirect conduction valleys.

Finally, it is worth mentioning that a special feature in the PL spectra from high-quality Ge is not yet understood. Liu *et al.* [102] reported an un-identified PL peak at 0.74 eV (Figure 12.14a–c). The temperature-independence of the peak position is distinctively different from the behavior of direct and indirect gap transitions in Ge. This transition dominates the PL spectra in the temperature range of 130–210 K. Its intensity decreases with the increase of temperature with a small activation energy of 56 meV (Figure 12.14d). Interestingly, when tensile strain is applied this peak shifts to the opposite direction of direct and indirect PL peaks (Figure 12.14e). This peak was observed in n-type, p-type, and intrinsic bulk single crystalline Ge alike. What is remarkable about this transition is that it is above the minimum band gap (indirect gap) of Ge, which means that the associated energy levels have to be inside the conduction or valence band. This above-band-gap transition has been observed in III–V semiconductors with dilute nitrogen doping as isoelectric centers, but it has never been reported in any group IV materials. While the origin of the transition needs further studies to identify, this observation may open a door to the further understanding of radiative transitions in Ge.

12.4.1.2 Spontaneous Emission from Ge and GeSn Microcavities

In recent years, there has been a lot of interest in studying light emission from microcavities due to their small footprint, potential for on-chip WDM laser banks, and spontaneous emission enhancement by the Purcell effect. Lim *et al.* reported enhanced emission at resonant wavelengths from intrinsic Ge-on-Si microring resonators ([103], Figure 12.15a). A quality factor of $Q = 620$ was achieved due to strong optical confinement, an order of magnitude higher than that previously reported on crystalline germanium microcavities. Shambat *et al.* [105] fabricated and optically characterized Ge-on-Si microdisks. The emission was coupled to a tapered fiber and multiple whispering gallery modes were observed. Cheng *et al.* [106] further demonstrated cavity modes in EL spectra from similar Ge-on-Si microdisks. However, in all these cases the Q factor decreases when pumping power or injection current is increased, indicating that there is no optical bleaching in these devices. This result is somewhat surprising considering that optical bleaching has been observed even in intrinsic unstrained bulk Ge [21] or GeOI [25]. The lack of bleaching in these Ge-on-Si microresonators could be due to two possible reasons: (i) defects introduced by fabrication. Reactive ion etching has been applied to fabricate microresonators in these cases, which could introduce defects on the sidewall that strongly interact with the whispering gallery modes. (ii) In the case of optical pumping, the pump lasers are typically in the visible regime. As we discussed earlier, such high-energy pumping photons are not favorable for direct gap transitions. Future investigations may elucidate the key to high performance Ge micro-resonator emitters.

Very lately, Ge/GeSn QW/Ge microdisk resonators have been fabricated and tested [104]. The 20 nm thick $Ge_{0.92}Sn_{0.08}$ QW is sandwiched by an ~100 nm thick Ge barrier layers on top and bottom, which are grown on 4 μm thick Ge buffer

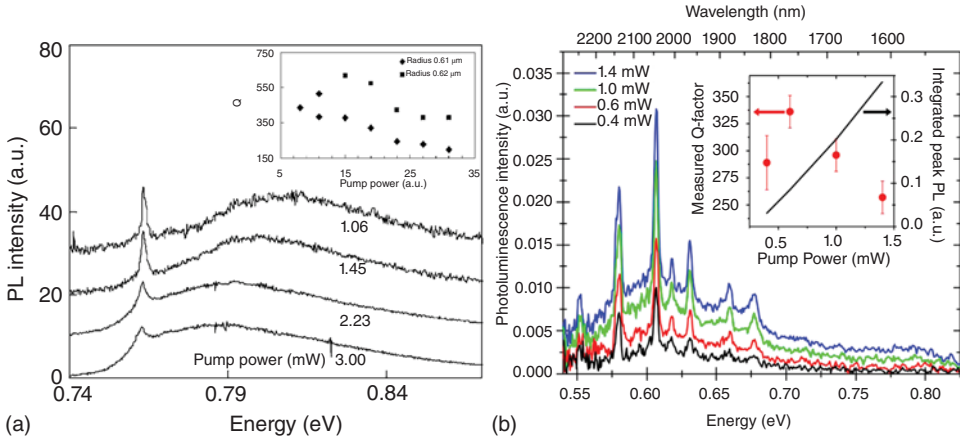

Figure 12.15 Pump power dependent PL spectra of (a) a Ge microring resonator with a radius of 0.61 μm. Reprinted from [103] with permission of AIP Publishing, LLC. (b) A $Ge/Ge_{0.92}Sn_{0.08}/Ge$ QW microdisk with a diameter of 2.7 μm. The peaks correspond to the whispering gallery modes in the resonators. The insets in both figures show the Q factor versus pump power. Reprinted with permission from [104]. © 2014 American Chemical Society.

layers on Si. Upon optical pumping at $\lambda = 980$ nm, clear resonant modes were observed around $\lambda = 2200$ nm (Figure 12.15b). As the pumping energy increases, the quality factor (Q factor) initially increases from 290 to 340, indicating optical bleaching. However, then the Q factor starts to decrease with pump power. Analysis shows that the decrease in Q factor is mainly due to the FCA losses in the Ge layers, considering that the optical confinement in the GeSn QW region is only 10%. With improved photonic structure design or pumping photon energy smaller than the indirect band gap of Ge, it could be possible to achieve net gain from the GeSn QW for microresonator laser applications.

12.4.2 Optical Gain

As we have discussed earlier, to achieve net optical gain Ge has to be band engineered by tensile strain and/or n-type doping to compensate the energy difference between its direct and indirect band gaps. Experimentally, optical gain was first observed from selectively grown, 0.25% tensile-strained n^+ Ge-on-Si mesas with n-type doping level of 10^{19} cm^{-3} and lateral dimensions <25 μm in pump-probe spectroscopy [107]. There are two major advantages in using selectively grown Ge mesas to investigate optical gain compared to blanket Ge films on Si: (i) the threading dislocation density is lower than in blanket Ge films as these dislocations can glide to the sidewalls of the mesas and annihilate [64]. Consequently, non-radiative recombination is effectively reduced. (ii) The SiO_2 mask layer for the selective growth naturally provides carrier confinement in the lateral directions to increase injected carrier concentration in the Ge mesa at a given pump power. A

CW 1480 nm pump laser was used in this study; therefore, all the optical bleaching and gain results are directly related to steady state pumping for device applications. The pumping photon energy is only 70 meV above the direct band gap so that the excitation condition is similar to electrical injection using heterojunction structures. The transmittance spectra of the probe laser through the thickness of the Ge mesa with and without optical pumping are shown in Figure 12.16a. A significant increase in transmittance upon optical pumping was observed at wavelengths above the direct gap transition (0.765 eV). To derive the absorption spectra of the sample with and without optical pumping from the transmittance data, transfer matrix method and Kramers–Kronig relation were applied to solve both the real refractive indices (n_r) and the absorption coefficients coefficient (α) by iterative self-consistency regression. The derived absorptions spectra with and without optical pumping are shown in Figure 12.16b. The absorption coefficients at photon energies >0.765 eV ($\lambda < 1620$ nm) decreases significantly upon optical pumping, corresponding to the transmittance increase in Figure 12.16a. Especially, negative absorption coefficients corresponding to the onset of optical gain are observed in the wavelength range of 1600–1608 nm. The shape of the gain spectrum near the direct band edge of Ge resembles those of III–V semiconductor materials. A gain coefficient of ~50 cm^{-1} was observed at 1605 nm. As we will show later, this optical gain supports optically-pumped Ge-on-Si lasers.

More recently, optical gain has also been reported in tensile-strained n^+ Ge photonic wires grown on GaAs [77]. The motivation of using GaAs substrate is that it has almost no lattice mismatch with Ge, thereby significantly improving the material quality of epitaxial Ge layers compared to Si substrate. The n-type doping level in Ge was 3×10^{19} cm^{-3}. A Si_3N_4 stressor with an initial compressive stress of 1.3 GPa was deposited and patterned to introduce tensile strain into the Ge layer. A maximum tensile strain of 0.6% was transferred to Ge at the SiN_x/Ge interface, while the average tensile strain in the Ge region is ~0.4%. An optical gain of 80 cm^{-1} at ~1685 nm was measured by variable strip length method. Emission line narrowing with increased optical pumping power was also observed.

Lange *et al.* [108] performed ultrafast pump-probe spectroscopy on intrinsic Ge/SiGe QW structures at low temperatures and reported transient gain on the order of several hundred cm^{-1} [108]. However, due to intervalley scattering from Γ to L valleys the gain lifetime is <100 fs. Note that in this case the Ge QWs are compressively strained, which increases the energy difference between Γ and L valleys and enhances the undesirable electron scattering from direct Γ to indirect L valleys. It is possible that the scattering rate can be improved with n-type doping and tensile-strain stressors to provide a longer gain lifetime, as suggested by the observation of the favorable L-to-Γ intervalley scattering in tensile-strained n^+ Ge discussed in Section 12.2.3 [37].

Wang *et al.* [109] investigated the *inherent* optical gain from the direct gap transition of wafer-bonded GeOI and epitaxial n^+ Ge-on-Si using femtosecond transmittance spectroscopy captured before the direct-to-indirect valley scattering. It was found that the inherent gain from the direct gap transition is 25 times larger than the steady-state gain in 0.25% tensile-strained Ge-on-Si with

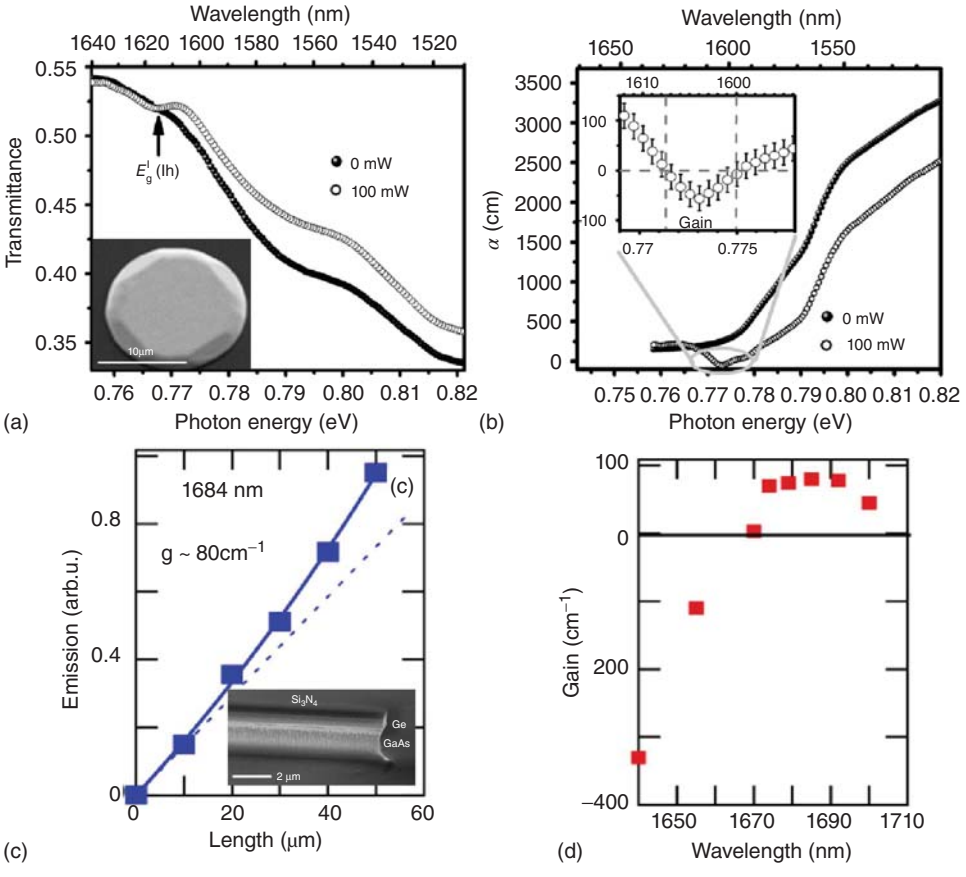

Figure 12.16 (a) Transmittance spectra of a 500 μm^2 Ge-on-Si mesa sample with $n = 1.0 \times 10^{19}$ cm^{-3} under 0 and 100 mW CW optical pumping at $\lambda = 1480$ nm. The inset shows an SEM picture of the mesa. (b) Absorption spectra of the n$^+$ Ge mesa sample under 0 and 100 mW optical pumping. Negative absorption coefficients corresponding to optical gain are observed in the wavelength range of 1600–1608 nm, as shown in the inset. Panels (a) and (b) are reprinted from [107] under the Author's Copyright Transfer Agreement with the OSA. (c) Edge emission intensity versus the length of the pumped region for a Ge/GaAs waveguide. The Ge layer has an n-type doping level of 3×10^{19} cm^{-3} and an average tensile strain of 0.4% transferred by a SiN stressor. An SEM image of the waveguide is shown in the inset. The superlinear increase of emission intensity with the length of pumped region indicates a gain of 80 cm^{-1} at $\lambda = 1684$ nm. (d) Gain spectrum of the Ge-on-GaAs waveguide structure. Panels (c) and (d) are reproduced from [77] with permission of the OSA.

$n = 1 \times 10^{19}$ cm^{-3}, suggesting that reducing $\Gamma \rightarrow$ L or enhancing L $\rightarrow \Gamma$ inter-valley scattering may significantly increase the optical gain of Ge lasers.

Carroll *et al.* [110] investigated optical gain from nominally unstrained intrinsic Ge, unstrained n$^+$ Ge ($n = 2.5 \times 10^{19}$ cm^{-3}), and 0.25% tensile strained intrinsic Ge on Si using 100 ps pump pulses at 1064 nm. Different from [77, 107, 111, 112],

the material was grown by low energy plasma enhanced chemical vapor deposition (LEPECVD) that tends to incorporate more hydrogen than UHVCVD and MOCVD. While the fitting to the experimental data revealed up to 850 cm^{-1} optical gain from the direct gap transition at a photon energy of 0.74 eV for $\Delta t = 0$, it was not large enough to overcome the pump-induced FCA losses. The authors concluded that net gain cannot be observed for nominally unstrained intrinsic Ge, unstrained n^+ Ge ($n = 2.5 \times 10^{19}$ cm^{-3}), or 0.25% tensile-strained intrinsic Ge on Si within the experimental error range of ± 50 cm^{-1}. This conclusion is largely consistent with the theoretical analysis in Figure 12.4a. The error range is comparable to the optical gain reported by [77, 107], though, so it may not be accurate enough to identify such a small gain near the direct band edge. It has been identified that FHA through *direct* inter-valence band transitions, for example, from the split-off band to the heavy hole band with the same k vector, was the major reason for carrier induced losses. A hole absorption cross-section of $\sigma_h = 3.8 \times 10^{-17}$ cm^2 was derived from the experimental data at $h\nu \sim 0.75$ eV. This cross-section is 12 times larger than the FEA cross-section, and it is within a factor of 2 compared to the FHA described by Eq. (12.6a). One possible reason for the difference is that the 1064 nm pumping light is not fully absorbed by the Ge thin films, so it can reach the Si substrate and generate additional free carriers to induce extra absorption. It is also possible that defect-assisted pump-induced absorption plays a role. Indeed, the same group reported a short carrier lifetime of 0.4 ns for Ge-on-Si with $n = 1 \times 10^{19}$ [95], while their UHVCVD counterparts showed a much longer lifetime of ~4 ns at the same doping level [113]. Improving material quality is always a critical factor for optical gain media.

12.4.3 Optically-Pumped Ge-on-Si Lasers

Based on the optical gain in band-engineered Ge-on-Si, an optically pumped Ge laser has been demonstrated at room temperature [111, 112]. The device consists of multimode Ge waveguides with mirror polished facets selectively grown on a lightly doped p-type Si wafer. The Ge material incorporates 0.24% thermallyinduced tensile strain and 1×10^{19} cm^{-3} *in situ* phosphorous doping. A cross-sectional scanning electron microscopy (SEM) image of the Ge waveguide is shown in the inset of Figure 12.17a. The length of the waveguides was 4.8 mm to guarantee a mirror loss of $\ll 10$ cm^{-1}, which is much smaller than the optical gain of Ge [107]. The entire waveguide was excited by a 1064 nm Q-switched laser with a pulse duration of 1.5 ns and a maximum output of 50 μJ per pulse. Figure 12.17a shows the light emission spectra of a Ge waveguide under different pumping levels. With the increase of pumping pulse energy, the spectrum evolved from a broad spontaneous emission band to sharp emission lines featuring stimulated emission. Correspondingly, the polarization evolved from a mixed transverse electric (TE)/TM to predominantly TE with a contrast ratio of 10 : 1 due to the increase of optical gain, as expected for typical lasing behavior. The multiple emission peaks at high pump power are due to multiple guided

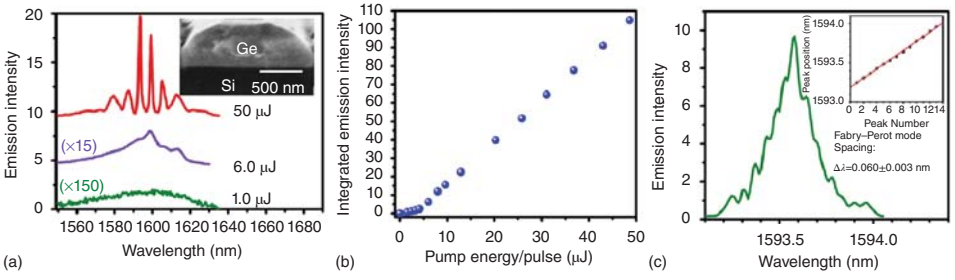

Figure 12.17 (a) Edge-emission spectra of a Ge-on-Si waveguide with mirror polished facets at different optical pumping levels. With the increase of pumping pulse energy the spectrum evolves from broad spontaneous emission to sharp lines of stimulated emission. The inset shows a cross-sectional SEM picture of the Ge waveguide. (b) Integral emission intensity from the waveguide facet versus optical pump power showing the lasing threshold. (c) High-resolution scan of the emission line at 1593.6 nm. Longitudinal Fabry–Perot modes are clearly observed, and the period is consistent with the Ge waveguide cavity length of 4.8 mm. Reprinted from [111] under the Author's Copyright Transfer Agreement with the OSA.

modes in the high index contrast Ge waveguide. A clear threshold behavior is demonstrated in Figure 12.17b. Figure 12.17c further shows a high resolution scan of the emission line at 1593.6 nm using a spectral resolution of 0.1 nm. Periodic peaks corresponding to longitudinal Fabry–Perot modes are clearly observed in the spectrum. The spacing of 0.060 ± 0.003 nm is in good agreement with the calculated Fabry–Perot mode spacing of 0.063 nm for a 4.8 mm-long Ge waveguide cavity.

12.4.4
Electrically-Pumped Ge-on-Si Lasers

Developing electrically-pumped Ge-on-Si lasers is the ultimate goal for practical applications. Ge-on-Si light emitting diodes (LEDs) based on direct gap transition have been demonstrated at room temperature since the late 2000s [47, 56–58]. However, electrical-pumping Ge-on-Si lasers pose two major challenges compared to optically pumped lasers: (i) higher material gain is required to overcome optical losses in heavily doped electrodes. Optically pumped lasers do not require any electrodes, so Ge waveguides can be grown on lightly doped Si substrate with negligible FCA loss in Si. Electrically pumped lasers, on the other hand, inevitably require heavily doped electrodes for current injection. For Si/Ge/Si double heterojunction (DH) structures, the FCA loss in heavily doped Si is $>100\,\mathrm{cm}^{-1}$ depending on the Ge thickness due to the modal overlap with the heavily doped Si. Further considering the mirror losses, practically a material gain coefficient of $\sim 200\,\mathrm{cm}^{-1}$ in the Ge active region is needed to achieve electrically pumped lasers. Therefore, n-type doping and/or tensile strain has to be increased to achieve this goal. (ii) High efficiency injection of holes into n^+ Ge needs to be achieved. Optical pumping naturally generates pairs of electrons and holes

simultaneously when an excitation photon is absorbed by Ge, so optical injection of electrons and holes is equally efficient regardless of the doping level. However, electrical injection of holes into a heavily doped n^+ Ge region is more challenging because the concentration of these minority carriers tends to decay rapidly with the distance from the junction due to recombination with electrons (majority carriers) in n^+ Ge. Adequate heterojunction structures have to be developed to overcome this issue.

Sun *et al.* [26] theoretically investigated electrical injection in 0.2% tensile-strained intrinsic and n^+ Ge with 1×10^{19} cm^{-3} dopant concentration using Si/Ge/Si DH structures. The modeling shows that the EL efficiency of n^+Si/n^+ Ge/p^+ Si DH LEDs is ~10%, two orders of magnitude higher than tensile-strained intrinsic Ge and comparable to their III–V counterparts. The estimate of efficiency enhancement by n-type doping is consistent with previous PL studies [44]. Liu *et al.* [92] further performed electrical injection modeling for n^+ Ge with a doping level of 5×10^{19} cm^{-3}, which can potentially achieve a net material gain of >200 cm^{-1}. It was found that although Si/Ge interface shows typical Type-II band alignment, the n^+ doping and applied forward bias creates a band bending that overwhelms the band alignment effect, resulting in a pseudo Type I alignment shown in Figure 12.18a. With 1.2 V (net) forward bias applied to the junction, the separation between quasi-Fermi levels of electrons and holes is larger than the direct band gap, which indicates that population inversion and optical gain can be achieved. Figure 12.18b shows that approximately 6×10^{18} cm^{-3} holes can be injected into the n^+Ge material at 1.2 V forward bias. These simulation results show that it is feasible to achieve efficient hole injection for electrically pumped optical gain using an n^+ Si/n $^+$Ge/p^+ Si DH structures.

The first electrically pumped Ge laser was based on an n^+ Si/n $^+$Ge/p^+ Si DH structure with an active n-type doping level of $>4\times10^{19}$ cm^{-3} [89, 114, 115]. To

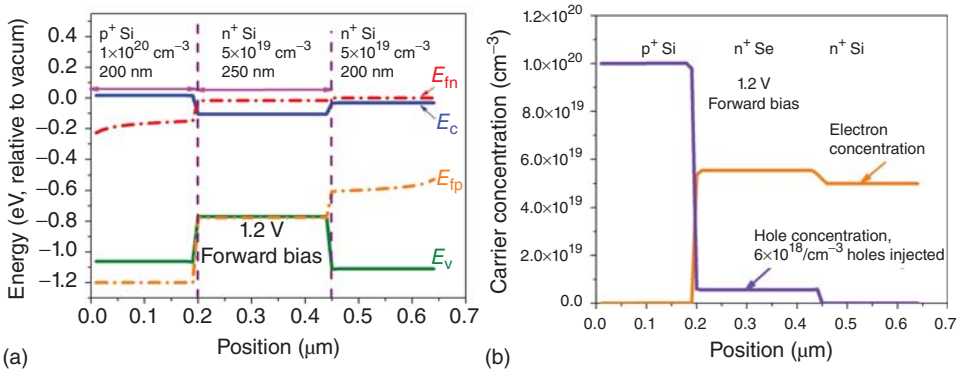

Figure 12.18 Electrical injection simulation of an n^+ Si/n^+Ge/p^+ Si double heterojunction structure. The doping levels and layer thicknesses are indicated in the figures. (a) Band diagram and quasi Fermi levels across the junction. Here, E_{fn} and E_{fp} stand for quasi Fermi levels of electrons and holes, respectively. (b) Carrier density distribution. Reprinted from [92], with permissions from Elsevier © 2012.

achieve this high doping level, the previously described delta-doping plus drive-in diffusion method was adopted. The stack of delta doped Ge was removed after the drive-in diffusion by CMP to eliminate the poly crystalline Ge. Fabry–Perot cavities were formed by selective Ge growth into SiO_2 openings of 1 µm width and various lengths up to several millimeters on the heavily n-type doped Si substrate. The Ge thickness varied throughout the wafer from 100 to 500 nm due to an inhomogeneous CMP process. SiO_2 was used to protect the Ge facets from catastrophic optical failure due to the high optical field during lasing operation. The top p^{++} Si contact of the DH structure was formed by the deposition of PECVD a-Si with subsequent Boron implantation. The top metal contact, consisting of a Ti–Al–Ti stack, covers the entire p^{++} Si to ensure reliable electrical injection into the Ge waveguide (see the inset of Figure 12.19a).

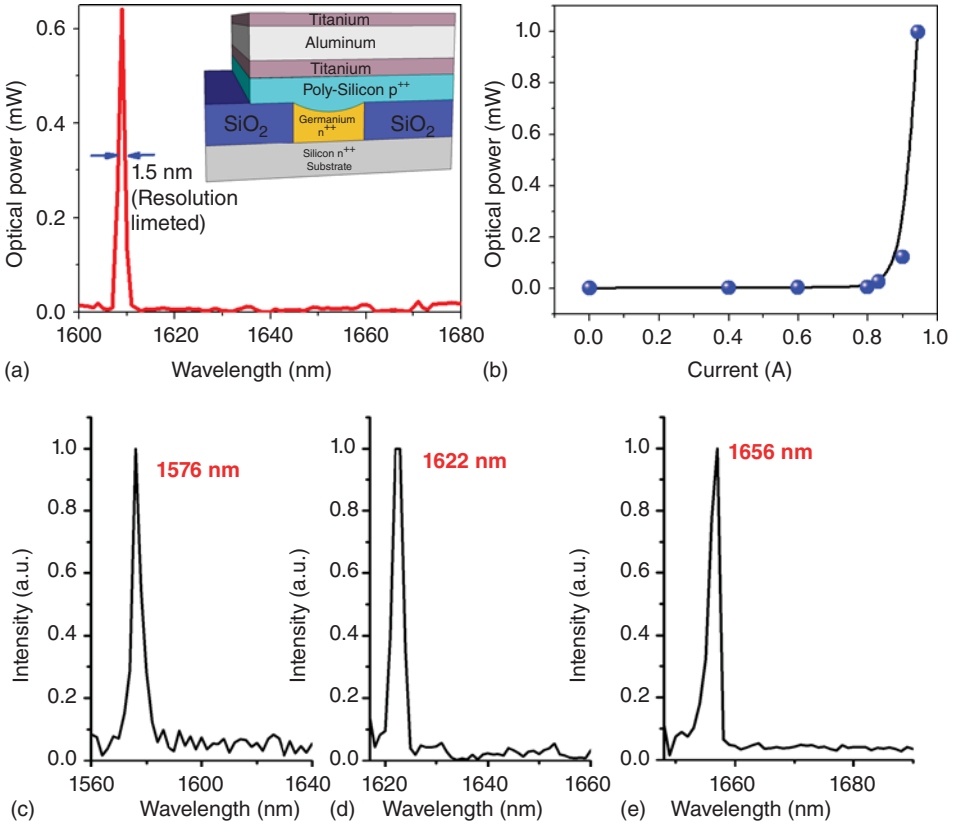

Figure 12.19 (a) A typical emission spectrum of an electrically pumped band-engineered Ge-on-Si laser diode. The inset schematically shows the cross-section of the device. The width of the Ge waveguide is 1 µm and the length is 270 µm. (b) L-I curve for the 270 µm long waveguide device. 40 µs electrical pulses were used at 1000 Hz. Spectra of Ge lasers with different Ge layer thicknesses are shown in (c–e). Reprinted from [89] with permission of OSA.

A pulse generator combined with a laser power supply was used to inject current into the Ge waveguide. By increasing the current density, a clear threshold can be observed when a sharp emission line with less than 1.2 nm linewidth appear. Figure 12.19a,b shows a representative emission spectrum and the corresponding L-I curve of an electrically pumped Ge-on-Si LD at room temperature, respectively. In this case, the output optical power is ~1 mW at an emission wavelength of 1610 nm. Depending on the thickness of the Ge layer and corresponding modal losses due to FCA in the electrodes, the clamping conditions of lasing vary accordingly and lasing wavelengths in a broad spectrum range of 1530–1700 nm have been observed (Figure 12.19c–e). Such a broad gain spectrum is consistent with the theoretical modeling we showed in Figure 12.4b that took into account the BGN effect and the FEA from first principle analyses. It also enables on-chip WDM when integrated with waveguide coupled Ge photodetectors [116] and modulators [117]. The observed maximum output power is 8 mW at room temperature.

A slope efficiency of $\eta_{slope} = 2\%$ was demonstrated in an un-optimized device structure (e.g., Figure 12.19b). We estimated an internal loss of $\alpha_i = 636\,cm^{-1}$ due to FCA (in both n^+ Ge region and the Si electrodes) and a mirror loss of $\alpha_m = 45\,cm^{-1}$ [39]. Therefore, the internal quantum efficiency (IQE) of this prototype Ge-on-Si diode is estimated to be

$$IQE = \eta_{slope}\left(\frac{\alpha_i + \alpha_m}{\alpha_m}\right) \sim 30\% \tag{12.12}$$

The major limiting factor of IQE is likely to be Auger recombination, which tends to be dominated by free holes in Ge. Therefore, reducing the required injected carrier density for transparency is the key to further increasing the efficiency.

Based on the results from the prototype device and the discussions in this chapter, there are a number of approaches to further enhance the performance of Ge LDs in future research. (i) Optimize the balance among tensile strain, n-type doping, and Sn alloying. As mentioned in Section 12.2.6, each of these methods has its own technical difficulties when used alone. However, one could utilize moderate levels of tensile strain, n-type doping, and Sn alloying to optimize optical gain and lasing without inducing significant challenges in materials growth and fabrication. Considering the reports of 5.7% uniaxial tensile strain, $>4 \times 10^{19}$ cm^{-3} n-type doping, and 9–10 at% Sn alloying achieved so far, there is a lot of room available for such optimization. For 0.25% tensile strained Ge, our simulations have shown that if the n-type doping is increased to $>7 \times 10^{19}\,cm^{-3}$ the threshold current density can be decreased below 1 kA cm^{-2} at 1600–1700 nm, comparable to III–V DH lasers [39]. If tensile strain is increased or Sn is incorporated, the n-type doping level can be further decreased and the performance improved. Interestingly, our optical gain simulations show that even for band-engineered Ge right at the indirect-to-direct transition point ($E_g^\Gamma = E_g^L$), having an n-type doping on the order of mid $10^{18}\,cm^{-3}$ still enhances the performance of the gain medium. As the detrimental intra-L-valley

FEA of n^+ Ge is an order lower than our original estimation, the increase of optical gain far exceeds that of FEA losses when n-type doping is incorporated in this case. Moreover, lower injected carrier density is needed to reach the same level of optical gain. Correspondingly, FHA and hole-hole-electron Auger recombination process – the most dominant loss mechanisms – are also greatly reduced. All these factors can further reduce the threshold current density and increase lasing efficiency. (ii) Buffer-less selective growth of high quality n^+ Ge in narrow trenches $\leq$1 μm in width, as discussed in Section 12.3.2.2. This method could prevent dopant segregation and improve the material quality at the Ge/Si interface, thereby enhancing the carrier injection efficiency in Ge LDs. (iii) Incorporating tensile strain and/or Sn into Ge QWs. As discussed in Section 12.2.7, the compressive strain in SiGe/Ge QWs as well as the quantum confinement effect itself increases the energy difference between the direct and indirect gaps of Ge QWs. Therefore, under these conditions SiGe/Ge QWs actually perform worse than bulk tensile-strained n^+ Ge in optical gain and lasing [39]. With the recent progress in tensile strain engineering, we proposed that tensile strain has to be incorporated into Ge QWs in order to counteract the detrimental effect of epitaxial compressive strain and the adverse quantum confinement effect in SiGe/Ge QWs. Our modeling shows that 0.3% tensile-strained Ge QWs with $n > 4.5 \times 10^{19}\,\mathrm{cm}^{-3}$ can potentially achieve a threshold of $\sim$500 $\mathrm{A\,cm}^{-2}$, comparable to the performance of III–V LDs. Further incorporation of Sn alloying offers another handle to optimize the gain and lasing performance from the QW structures. In this case, the energy gap reduction due to tensile strain and Sn alloying can also be partially compensated by the quantum confinement effect. This helps to avoid potential issues related to the leakage current and enhanced Auger recombination in small band gap semiconductors. (iv) Separate confinement of Γ versus L electrons in QW structures. As mentioned in Section 12.2.7, by adequately designing the band alignment between the barrier and Ge QWs, one can enforce more quantum confinement for the L electrons (deeper well) versus the Γ electron (shallower well), thereby transforming Ge toward a direct gap semiconductor. This approach overcomes the existing issue of SiGe/Ge QWs. One would prefer to use direct gap barrier layers such as AlGaAs to implement such structures effectively. Although using III–V materials for an active region is a significant challenge in CMOS compatible fabrications, using them as barrier layers does not require such high material quality and may allow low-temperature, CMOS compatible fabrications.

Another interesting topic to explore is the optimal relative positions of L versus Γ valleys for on-chip laser sources without active cooling [54]. As mentioned in Section 12.4.1, a pseudo-direct gap configuration can enhance the direct gap emission efficiency at high temperature and high injection levels due to enhanced L-to-Γ valley excitation or scattering. Considering that the Auger recombination rate in indirect valleys is orders of magnitude smaller than the direct valleys due to the momentum mismatch, the same reason as its lower radiative recombination efficiency, it may be beneficial to "store" the injected electrons in the L-valley and supply it to the direct Γ valley using the fast intervalley scattering process

(sub-ps). This approach helps to optimize the efficiency as well as the high temperature performance of the band-engineered Ge LDs. Recent progress in Sn alloying and tensile strain will allow us to systematically change the relative energy positions between L and Γ valleys for this investigation. It is also important to study the Auger recombination process in these materials. Spectrally resolved ultrafast pump-probe measurements will likely provide important fundamental information on this aspect, especially distinguishing different processes during the relaxation of the injected carriers.

12.5 Conclusions

This chapter reviews the research on direct gap light emission and optical gain from Ge, including historical aspects, theoretical modeling, band-engineering approaches, spontaneous emission, and stimulated emission under optical and electrical pumping. The demonstration of electrically pumped monolithic Ge-on-Si lasers and the rapid progress in the experimental implementation of band-engineering approaches both point to promising future applications in large-scale, high volume electronic–photonic integrated circuits with on-chip WDM to multiply the capacity of photonic datalinks.

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